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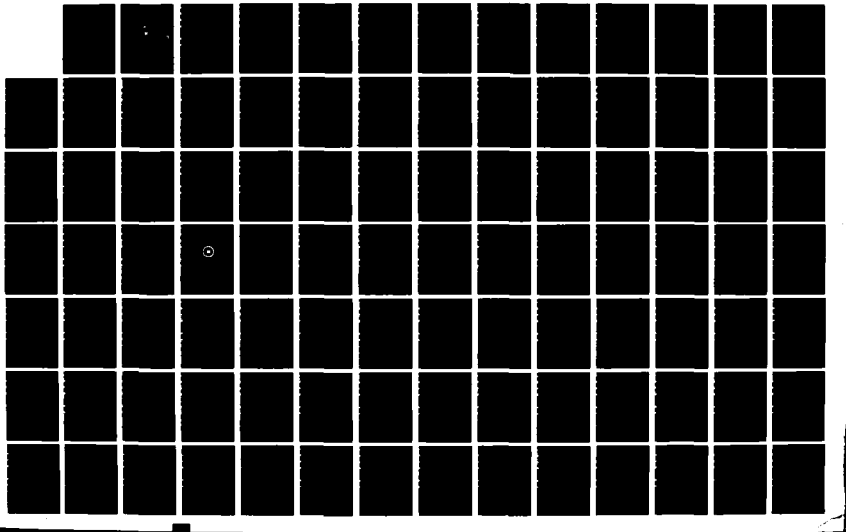

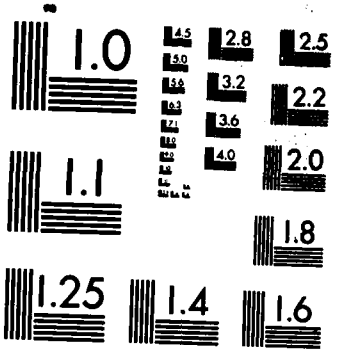

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

ELECTRON IRRADIATION OF N CHANNEL
SILICON ON SAPPHIRE INSULATED GATE
FIELD EFFECT TRANSISTORS (IGFET)

by

Robert A. Pornaras

December 1985

Thesis Advisor: K.C. Dimiduk

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sixty-five percent of its pre-irradiation value within thirty hours. It then increased slowly to about seventy-five percent of its pre-irradiation value by the end of the observed annealing time. Threshold voltage rebound was not observed. Saturation transconductance, device gain, increased initially above its pre-irradiation value. Irradiation at doses of 10^5 Rads (Si), or greater, caused the device gain to decrease from the peak value until it was about eighty percent of its pre-irradiation value at the maximum dose. A method for obtaining useful back- channel leakage current data is presented.

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Electron Irradiation of N Channel Silicon on Sapphire Insulated Gate Field Effect Transistors (IGFET)

by

Robert A. Pornaras
Lieutenant Commander, United States Navy
E.E., University of Washington, 1977

Submitted in partial fulfillment of the
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ABSTRACT

SOS, n-channel, insulated gate field effect transistors (IGFETs) were irradiated at room temperature with a 30 MeV electron beam at doses from 10^4 to 10^6 Rads (Si). The effects of the irradiation on IGFET performance were evaluated by measuring threshold voltage, saturation transconductance and leakage current. Threshold voltage decreased after each irradiation, up to the highest dose. The threshold voltage behavior was as expected for an n-channel IGFET undergoing gate oxide charge build-up. The total dose was not large enough to exhibit threshold voltage increases indicative of interface state generation. The IGFETs were allowed to anneal for 107 hours at room temperature. The threshold voltage recovered to approximately sixty-five percent of its pre-irradiation value within thirty hours. It then increased slowly to about seventy-five percent of its pre-irradiation value by the end of the observed annealing time. Threshold voltage rebound was not observed. Saturation transconductance, device gain, increased initially above its pre-irradiation value. Irradiation at doses of 10^5 Rads (Si), or greater, caused the device gain to decrease from the peak value until it was about eighty percent of its pre-irradiation value at the maximum dose. A method for obtaining useful back-channel leakage current data is presented.

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Finally, I would like to thank Dr. Ron Reedy of Naval Ocean System Center for providing the SOS devices and the requisite knowledge for their operation.

I. INTRODUCTION

The sophisticated weaponry, complex electronic components and interconnected communication systems used in many military and civilian applications depend upon the semiconductor, integrated circuit. These electronic systems must have the ability to perform in hostile radiation environments, both natural and man-made. The "hostile environment" not only refers to nuclear weapons but also nuclear reactors and space applications. To meet these requirements, a wide variety of electronic systems must be "hardened" to radiation.

Radiation "hardening" refers to making electronic devices and systems less susceptible to damage or upset from radiation. Table 1-1 [Ref. 1] shows the various radiation sources that can cause radiation damage in electronic devices. Much research has been done to determine the effects of different types of radiation sources on semiconductor materials.

The three major radiation sources are: (1) charged particles (ions, electrons, protons); (2) neutral particles (neutrons); and (3) photons (gamma rays, x-rays).

Ionization is the major damage mechanism of photons and charged particles. When applied in equal doses (measured in Rads (Si)), photons and charged particles cause equal

TABLE 1-1. RADIATION SOURCES

Sources	Radiation	Output
Natural Radioactive Material		
Uranium, Radium, Radon	alpha, beta, gamma	2.3 rads/hr
Irradiated Materials		
Cobalt-60, Sodium, Iodine	alpha, beta, gamma	to 10^{7} rads/hr
Fission Fragments		
Strontium, Cesium	alpha, beta, gamma	10^{9} rads/hr and up
From Space		
Cosmic radiation	nuclei	2 particles/cm²-sec (kinetic energies of 1 to 10 BeV)
Solar Flares	protons	1000 rads/hr
Van Allen Belts	electrons	10 rads/hr
Reactors	gamma	10^{7} rads/sec
	neutron	$\approx 10^{15}$ neutrons/cm²-s
Fission/Fusion Weapons (Percentage of weapon output)	alpha, beta	27.5%
	gamma	0.5%
	neutrons	2.0%
	x-rays	70.0%

amounts of ionization damage to a semiconductor material [Ref. 2]. Srour et al. [Refs. 3 and 4] and Cleveland [Ref. 5] found the dose rate to be an important factor when considering the effects of total dose on semiconductors. It

the same total dose is applied at different dose rates different amounts of damage can result. The permanent damage from ionizing radiation is discussed in Chapter II. Ionizing radiation causes induced trapped charge and interface states at the silicon-insulator boundary.

The chief damage mechanism of neutrons is displacement of the lattice atoms. Displacement alters the crystal structure of the material changing the minority carrier lifetimes in semiconductor materials.

A. OVERVIEW

Radiation hardening of semiconductors often requires special processing and/or special geometry for the device layout [Ref. 6]. The special processing and geometric layouts require added steps in the manufacturing process increasing the cost of the device. Elaborate geometric layouts decrease the packing density on the semiconductor chip. Decreasing the density increases the cost per device.

A manufacturing technique is required that will "harden" semiconductor devices without severely decreasing packing density or adding processing steps. The requirement is that the hardened semiconductor device be economical for civilian and military use. Naval Ocean Systems Center (NOSC), San Diego, California has developed a silicon-on-sapphire semiconductor device to meet the challenge of an economical yet "hard" semiconductor [Ref. 7].

The focus of this thesis centers on the results of irradiation of the n-channel SOS devices manufactured by NOSC. An electron beam linear accelerator was used as the irradiation source.

During the experiment completed for this thesis, n-channel SOS devices were irradiated using the Naval Postgraduate School (NPS) Linear Accelerator (LINAC). The changes in device characteristics (threshold voltage, saturation transconductance and leakage current) were monitored after irradiation. Changes in device characteristics measured the device response to total dose. This thesis will center on a discussion of the radiation effects due to total dose.

B. BACKGROUND

Development of SOS technology began in 1974. Limited production radiation-hard SOS devices manufactured by R.C.A. were available by 1977. G.E. and Hughes did research on SOS devices for use in computer memories and microprocessors. SOS technology offered greater potential for higher speed and density than bulk silicon technology [Ref. 8].

Early attempts to use SOS technology required a high degree of versatility on the part of circuit designers. Leakage current, threshold voltage, and carrier mobility vary widely from chip to chip and presented circuit design limitations [Ref. 9]. Technologies that did not have these

limitations soon replaced SOS technology in studies concerned with radiation hardened circuits.

Recent advancements have been made in material science leading to consistancy in SOS chip parameters. These advancements have rekindled an interest in SOS technology as a technique to produce radiation hard circuits.

C. PREVIOUS RESEARCH

Insulated gate field effect transistors (IGFETs) use a capacitor action across the gate oxide insulator for operation. Changes introduced in the insulator material or the underlying silicon gate channel region change the IGFET operating characteristics.

Operating characteristics can be carrier mobility, recombination time, threshold voltage, or any of the other parameters of a semiconductor device. The important operating characteristics are a function of the scale chosen. The parameters a circuit designer uses are device gain, leakage current and threshold voltage. These parameters are the ones used in this thesis to characterize device operability.

SOS devices differ from bulk silicon devices only in the substrate material. The numerous radiation studies on n-channel, insulated gate field effect transistors can be used to characterize the effects of radiation on SOS devices. The occurrence of a significant ionizing radiation

induced back-channel leakage current in n-channel SOS transistors is addressed as a separate problem [Ref. 4].

Srour et al. [Ref. 3] gives a review and critical evaluation of the research done on oxides and semiconductors through 1974. The report states that ionizing radiation causes an unacceptably large threshold voltage shift in semiconductor devices. This shift is due to a charge build-up in the gate oxide and the introduction of interface states at the silicon-oxide boundary. The large threshold voltage shift was determined to be the limiting parameter for device performance.

Threshold voltage is the gate voltage required to activate the transistor. The exact amount of threshold voltage shift that can be tolerated is a function of device application. A change of more than fifty per cent in threshold voltage is unacceptable for most transistor applications due to biasing considerations.

Srour et al. [Ref. 4] investigated the occurrence of back-channel leakage current peculiar to SOS devices. Back-channel leakage current reached a saturation level at approximately 10^{7} Rads (Si) from a Co^{60} source. Back-channel leakage current was able to be returned to its pre-irradiation value. Srour accomplished this by continued irradiation of the SOS device with drain-to-source voltage set to zero volts (ground). In the first irradiation, 5 volts was used for the drain to source voltage.

The damage produced in the IGFET by ionizing radiation may anneal out with time. Srour et al. found [Ref. 3] annealing to be a function of temperature and applied voltage. Annealing does not always return the device to its original condition (See Chapter II for further explanation).

A variety of research has been completed on annealing and damage processes for many devices, covering a range of applications. For the interested reader, the most recent review of the field is contained in the IEEE Nuclear and Space Radiation Effects Conference (NSREC) Short Course for 1985.

D. ORGANIZATION OF THESIS

The remainder of the thesis will be organized as follows. Chapter II presents a brief review of insulated gate field effect transistors (IGFETs) and the radiation damage mechanisms applicable to them. Electron radiation effects on matter and dose are also covered. Chapter III describes the equipment hook-up and computer programs used for data collection. The linear accelerator and semiconductor chip design parameters are described. A description of the methods used to characterize device performance is presented. Chapter IV is the analysis of the collected data with the raw data in Appendix D. Chapter V discusses the results and has suggestions for future studies.

II. THEORY

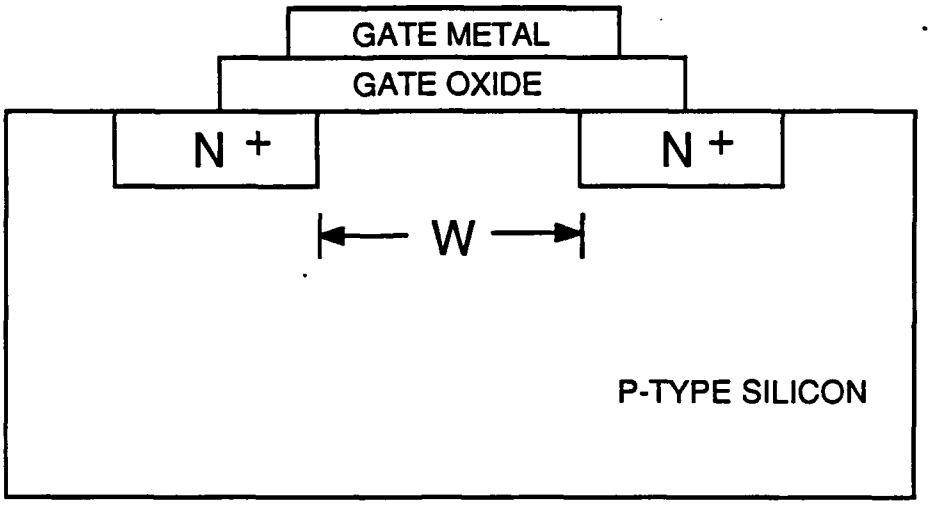
A basic radiation and insulated gate field effect transistor (IGFET) theory will be presented with the idea of giving a common basis for discussion. Since n-channel IGFETs are the devices used in this thesis, the IGFET devices referred to will be n-channel devices unless otherwise stated. The radiation damage will refer to electron beam effects and doses which, as pointed out in Chapter I, can be correlated to gamma and proton doses in a target material. The dose rate, gamma-dot, effects will be addressed only when required since total dose is the major concern in a single, unpaired, IGFET device.

A. IGFETs

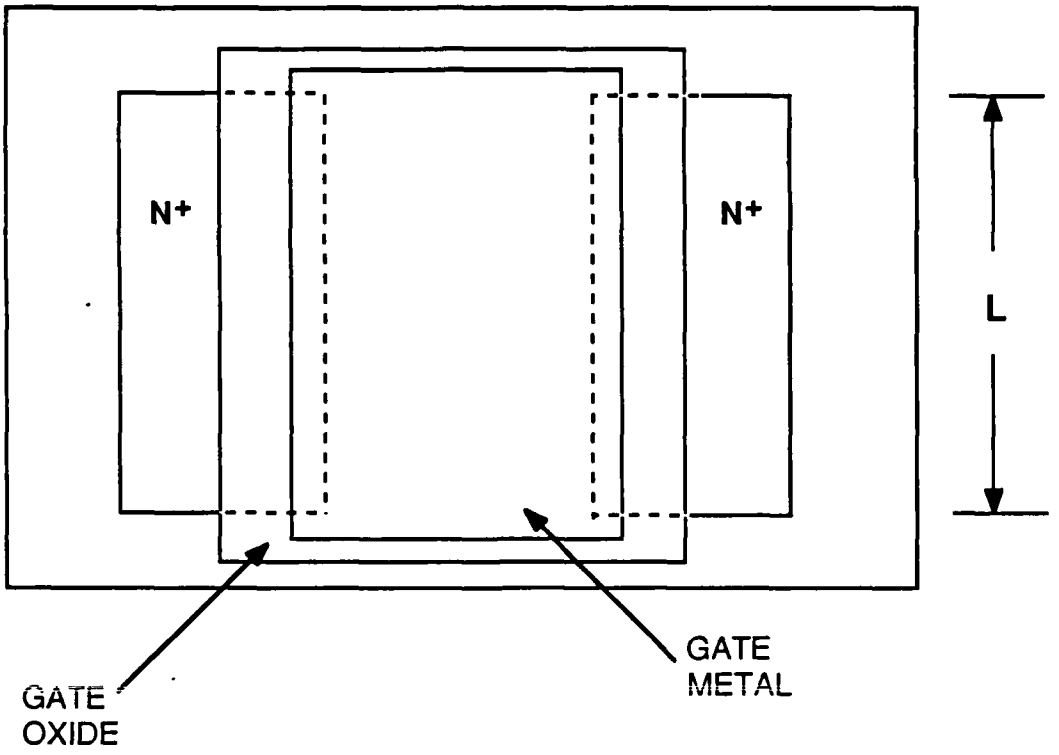
Integrated circuit (IC) devices are more than one device placed on a single semiconductor chip. The devices could be transistors, capacitors, resistors, diodes, etc., or any combination of these. The particular type of device used for this thesis is the n-channel, insulated gate field effect transistor (IGFET).

1. The N-Channel IGFET

The basic structure of an n-channel IGFET is shown in Figure 2-1. As can be seen in Figure 2-1a, the source and drain are electrically disconnected unless there is an



a) **Cross Section**



b) **Top View**

Figure 2-1 IGFET Layout Diagram.

n-type inversion layer along the oxide-silicon interface providing a channel for electron conduction. The ratio of channel width, W, to channel length, L, will be an important quantity in the equations describing IGFET parameters. There are three major technologies used for IGFETs: bulk silicon (Figure 2-2a); silicon-on-insulator (SOI) (Figure 2-2b); and silicon-on-sapphire (SOS) (Figure 2-2c). Both n- and p-channel devices are shown for comparison.

2. IGFET Parameters

The primary equation that will be used for the investigation of IGFET parameters is the equation for saturation drain current, I_{Dsat}, as developed in Reference 10, and given by:

$$I_{Dsat} = K' (W/L) (Vg - Vs - V_t)^2 \qquad (2\text{-}1)$$

where,

K' is proportional to μC_{ox} but, in general, is smaller than this product [Ref. 10].

C_{ox} = oxide capacitance per unit area

μ = channel charge mobility

Vg = gate voltage

Vs = source voltage

V_t = threshold voltage

The parameters that will be ideally modeled from Equation 2-1 and be used to characterize the operation of

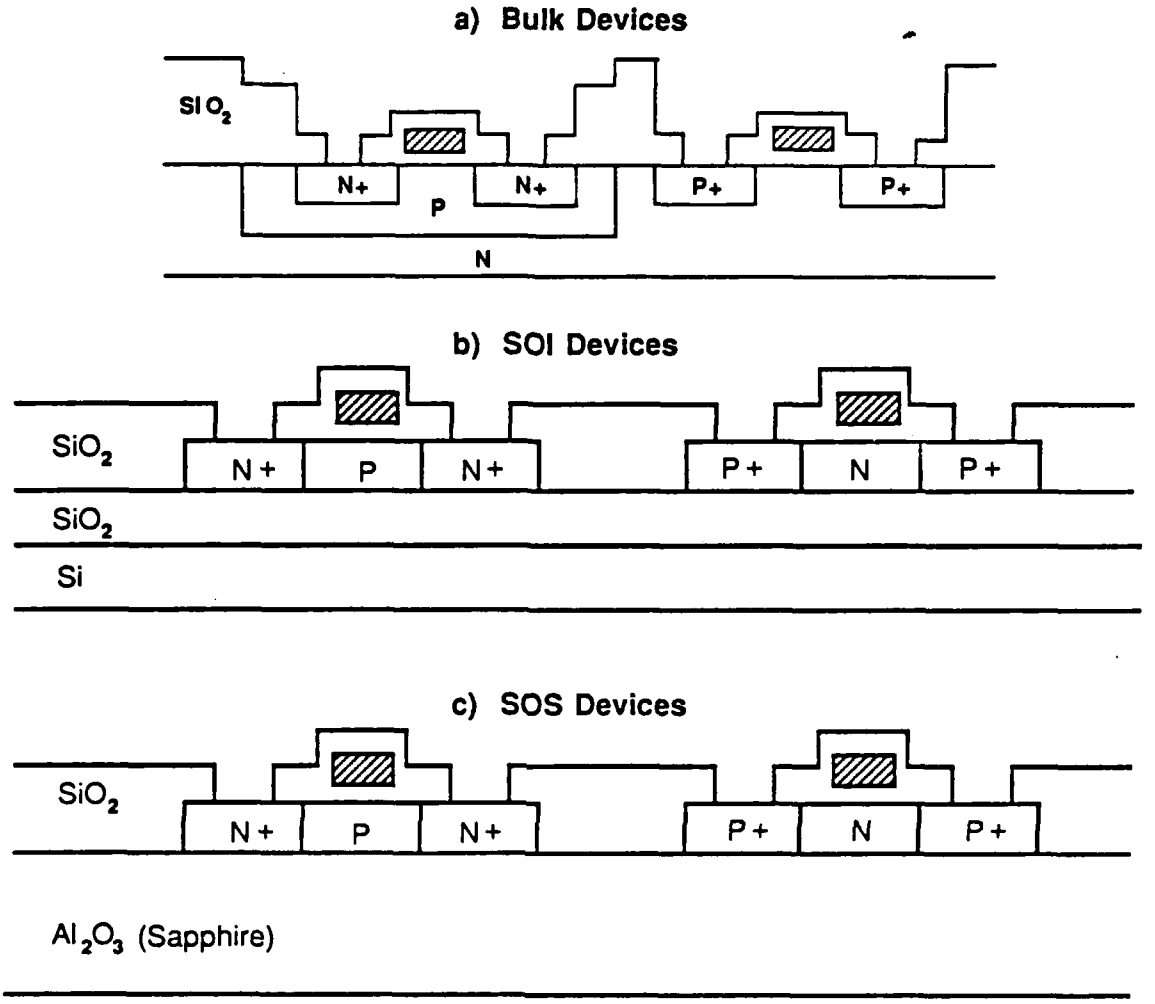


Figure 2-2 Silicon IGFET technologies. N- and p-channel transistors (left- and right-hand devices respectively).

the IGFET will be threshold voltage, V_t; transconductance, g_m; and leakage current. A method frequently employed to obtain the first two of these parameters is to tie together the gate and the drain of the transistor, Figure 2-3, and then measure drain current as a function of applied drain voltage as described below.

a. Threshold Voltage

With the substrate grounded, Vs=0, and the gate and drain tied together, V_D=Vg, it is apparent from Equation 2-1 that a plot of the square root of the drain current versus drain voltage will be linear. The threshold voltage is easily obtained by extending the linear portion of the curve back to the voltage axis and taking the intercept, as shown in Figure 2-4. The actual curve varies from the ideal linear curve modeled from Equation 2-1 because of the non-ideal behavior introduced by the free carriers in the gate-channel region. These free carriers cause a "leakage current" to flow below the conventional threshold voltage.

b. Transconductance

The transconductance is defined as:

$$g_{m\,sat} \equiv \frac{d(I_{D\,sat})}{dVg}$$

which, from Equation 2-1, gives:

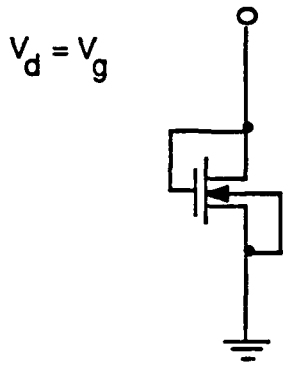


Figure 2-3 IGFET electrical connections for device parameter measurement.

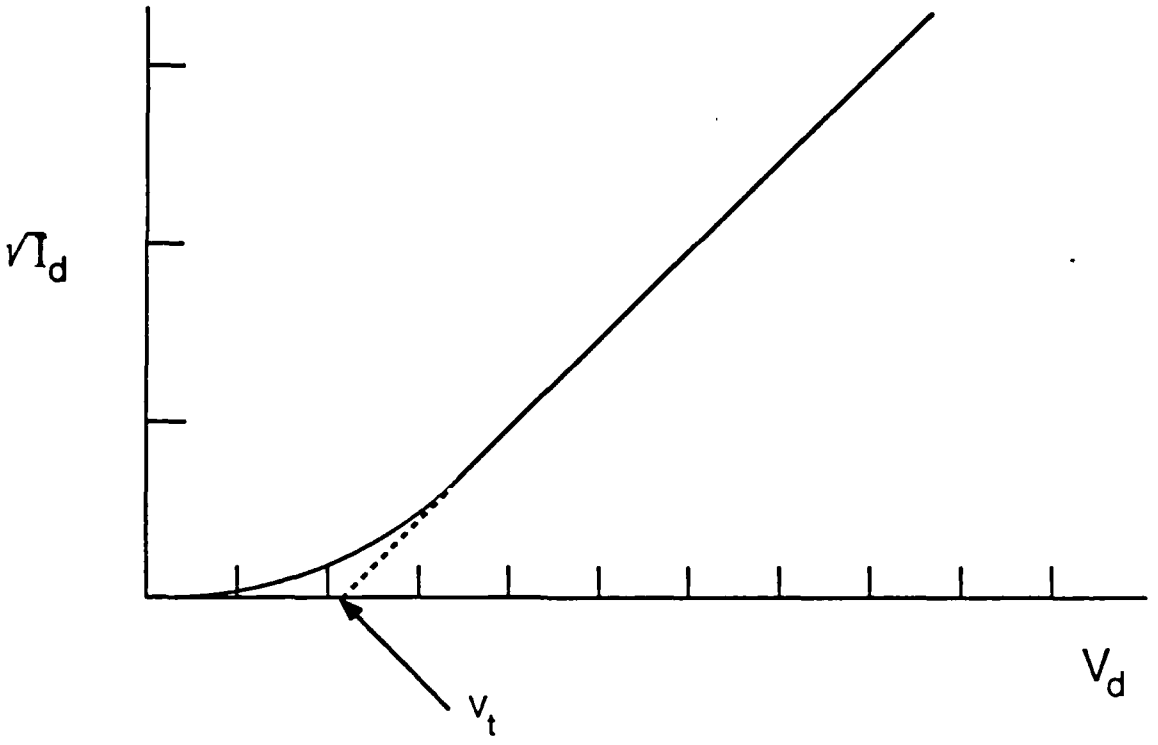


Figure 2-4 Graph of sample data for determining transconductance and threshold voltage. The saturation transconductance is calculated from the slope of the linear portion of the curve as explained in the text.

$$g_{msat} = 2K' (W/L) (Vg - Vs - V_t) \qquad (2\text{-}2a).$$

The slope of the curve in Fig. 2-4 can be used to determine K'(W/L). g_{msat} also depends upon the selection of the gate and source voltages. Selecting Vs = 0 and Vg = V_t + 0.5 in Equation 2-2a eliminates all the unknowns in the equation by selecting typical gate and source voltages and gives the form of the equation which will be used for calculating transconductance:

$$g_{msat} = K' (W/L) \qquad (2\text{-}2b).$$

c. Leakage Current

Gate voltages below the threshold voltage should ideally cut-off current flow in the transistor. However, current does flow due to inversion charge that exists at gate voltages below the threshold [Ref. 10]. This is a leakage current which can be measured directly.

B. ELECTRON RADIATION DAMAGE

A brief description of the types of radiation damage caused by high energy electrons in matter and the method of measurement of the amount of damage (dose) will be presented in this section.

1. Interaction of Electrons With Matter

As electrons making up a high energy electron beam pass through a target material, the primary interaction is inelastic Coulomb scattering. The electrons lose energy in the scattering process through both ionization and bremsstrahlung [Ref. 11]. The amount of material required to cause a given energy loss is a measure of the stopping power of the material. Stopping power is defined as the amount of energy lost by a particle per unit length of path through the stopping material [Ref. 12]. The high energy particles will follow a straight line in the original direction of the incoming beam until the electron energies are diminished to some low level. At these lower energies, the electrons will be deflected through a broader angle giving a more defuse beam.

a. Electron Elastic Collision

Elastic scattering of the incident high energy electron, as a result of electron-nucleus collision, imparts some of the electron's kinetic energy to the nucleus, or atom. The recoiling atom then interacts with the surrounding atoms, transferring energy from the atom to the rest of the lattice. If the energy of the primary recoiling atom is low, all that results is heating of the crystal lattice. However, as the energy of the recoil atom increases, a threshold energy is reached (15.9 eV for silicon) where the recoil atom is ejected to an

interstitial site leaving a vacancy behind. At even higher energies, the recoil atom can have sufficient energy to displace other atoms which, in turn, can displace even more atoms in a cascading, billiard ball, fashion. This produces displacement/Frenkel defects [Ref. 13]. The amount of energy that can be transferred in this manner is highly dependent upon the mass ratios of the particles involved and is therefore very small for the electron-nucleus collision. Also, displacement damage primarily affects minority carrier lifetimes which, as will be discussed later, have little affect on the devices used for this thesis. For these reasons, radiation damage from elastic collisions will not be considered significant in this thesis and is discussed here for completeness only.

b. Electron Ionization/Collision Stopping Power

Ionization, or collision, stopping power is the inelastic collision of the beam electrons with the atomic electrons of the target material. Usually, inelastic collisions with atomic electrons result in excitation or freeing of the atomic electrons. See Figure 2-5.

The stopping power for inelastic collisions with atomic electrons is given by [Ref. 14]:

$$\left.\frac{1}{\rho}\frac{dE}{dx}\right|_{col} = \frac{2\pi N r^2 mc^2 Z}{\beta^2 A}\left[\ln\left(\frac{T}{I}\right)^2 + \ln(1+\tau/2) + F(\tau) - \delta\right] \qquad (2\text{-}3)$$

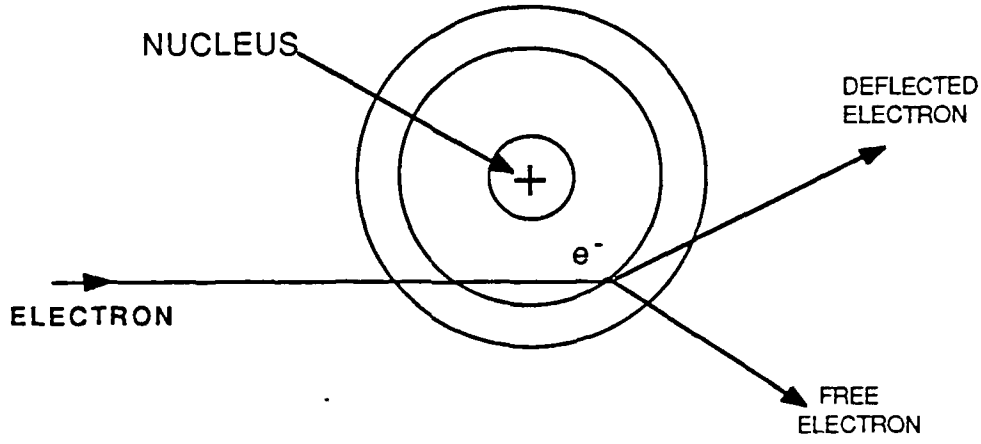


Figure 2-5 Freeing of an electron by inelastic collision of a beam electron with a target, atomic electron.

where,

ρ = Material density

N = Avogadro's number

r^2 = Square of the classical electron radius

mc^2 = Electron rest energy

Z = Atomic number

β = (electron velocity/velocity of light)

A = Atomic weight

I = Mean excitation energy in MeV

(The experimentally obtained mean excitation energies for a variety of elements can be found in tables [Ref. 14].)

T = Kinetic energy of electrons in MeV

$\tau = T/mc^2$

$F(\tau) = (1-\beta^2)\,[1 + (\tau^2/8) - (2\tau+1)\ln 2]$

δ = Density-effect correction [Ref. 14]

The above equation is derived from the Bethe theory using the Møller cross section (1932) and elaborations of Rohrlich and Carlson (1953), and Uehling (1954). The formula takes into account the electron cross sections for the target electrons, relativistic effects, and the density of the target electrons with their screening effect on the other electrons.

The tabulated value of the collision stopping power for 30 MeV electrons in silicon is 1.809 MeV-cm^2/g [Ref. 14].

c. Electron Radiative/Bremsstrahlung Stopping Power

It is a common phenomenon in electro-magnetism that when a charged particle is accelerated it radiates. When the beam electrons undergo an inelastic Coulomb collision with the nucleus, or the atomic electrons, of the target atoms, their direction of travel is changed and they radiate as shown in Figure 2-6. This radiation represents an energy decrease for the beam electrons and is called bremsstrahlung radiation. The radiative stopping power of a material is given by [Ref. 14]:

$$\left.\frac{1}{\rho}\frac{dE}{dX}\right|_{rad} = \frac{N}{A}\alpha r^2 E Z^2 \phi_{rr}[1 + (1/Z)(\phi_{re}/\phi_{rr})] \qquad (2\text{-}4)$$

where,

$\alpha = Z/137$

$E = T + mc^2$

ϕ_{rr} = dimensionless, scaled, radiative energy-loss cross section for electron-nucleus interaction.

ϕ_{re} = dimensionless, scaled, radiative energy-loss cross section for electron-electron interaction.

ϕ_{re}/ϕ_{rr} is assumed to be one

ϕ_{rr} values are aproximated from least-squares curves fitted from theoretical points based on the high energy theory of Davies, Bethe and Maximon [Ref. 14].

The tabulated value of the radiation stopping power for 30 MeV electrons in silicon is 1.108 MeV-cm^2/g [Ref. 14].

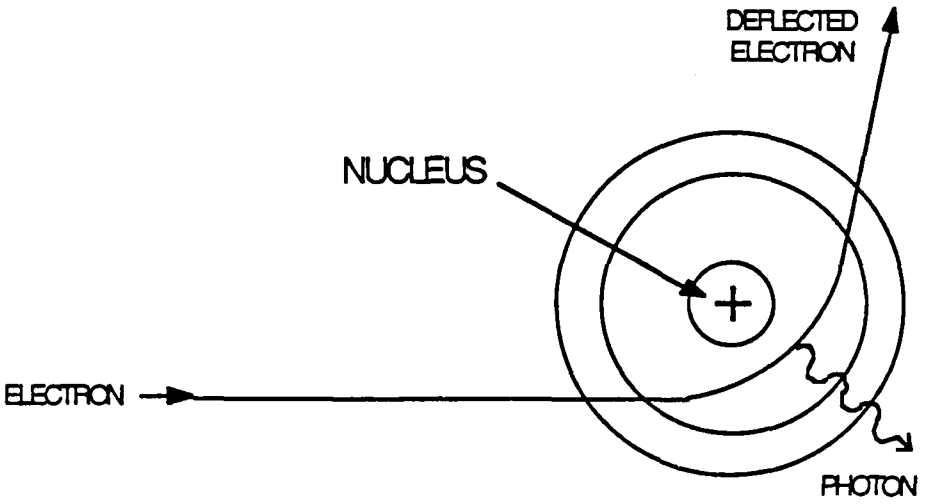


Figure 2-6 Creation of a photon by bremsstrahlung.

2. Damage Parameters

a. Range

Range is defined as the path length an electron travels while being brought to rest in a material. It is expressed in grams per square centimeter [Ref. 11]. The electrons are assumed to lose energy continuously as they come to rest. If the range is divided by the density of the target material, the most probable distance an electron can travel will be determined. For 30 MeV electrons in silicon the range is 13.83 g/cm^2 with the most probable distance traveled being 5.94 cm.

b. Dose

Dose represents the amount of energy deposited in the material. It is expressed in rads (100 ergs/gram) if one square centimeter of surface area is assumed and the particular material is specified. The front surface (thin sample) dose will be used in this thesis because, as can be seen in Figure 2-7, the electron beam is virtually unaffected, and therefore constant, in its passage through the target material. Also, the energy going into the ionization and excitation of atoms is absorbed in the medium rather close to the electron track, whereas most of the energy lost in the form of bremsstrahlung travels far from the track before being absorbed. Therefore, since dose is the amount of energy deposited in the material, the

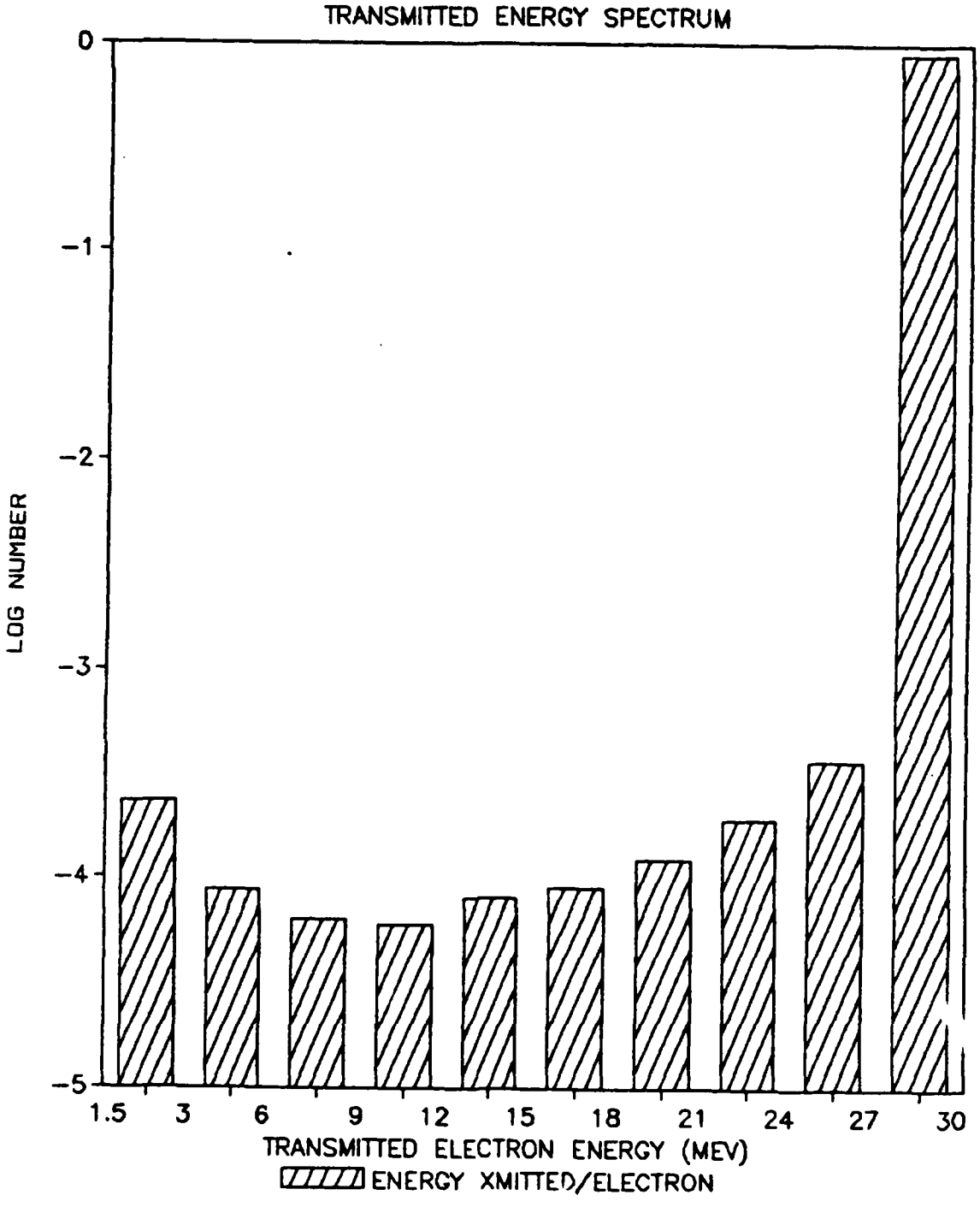


Figure 2-7a. Computer simulation of the energy spectra for electrons transmitted through 30 mil thick Al_2O_3 (sapphire). Spectra is normalized to one incident 30 MeV electron.

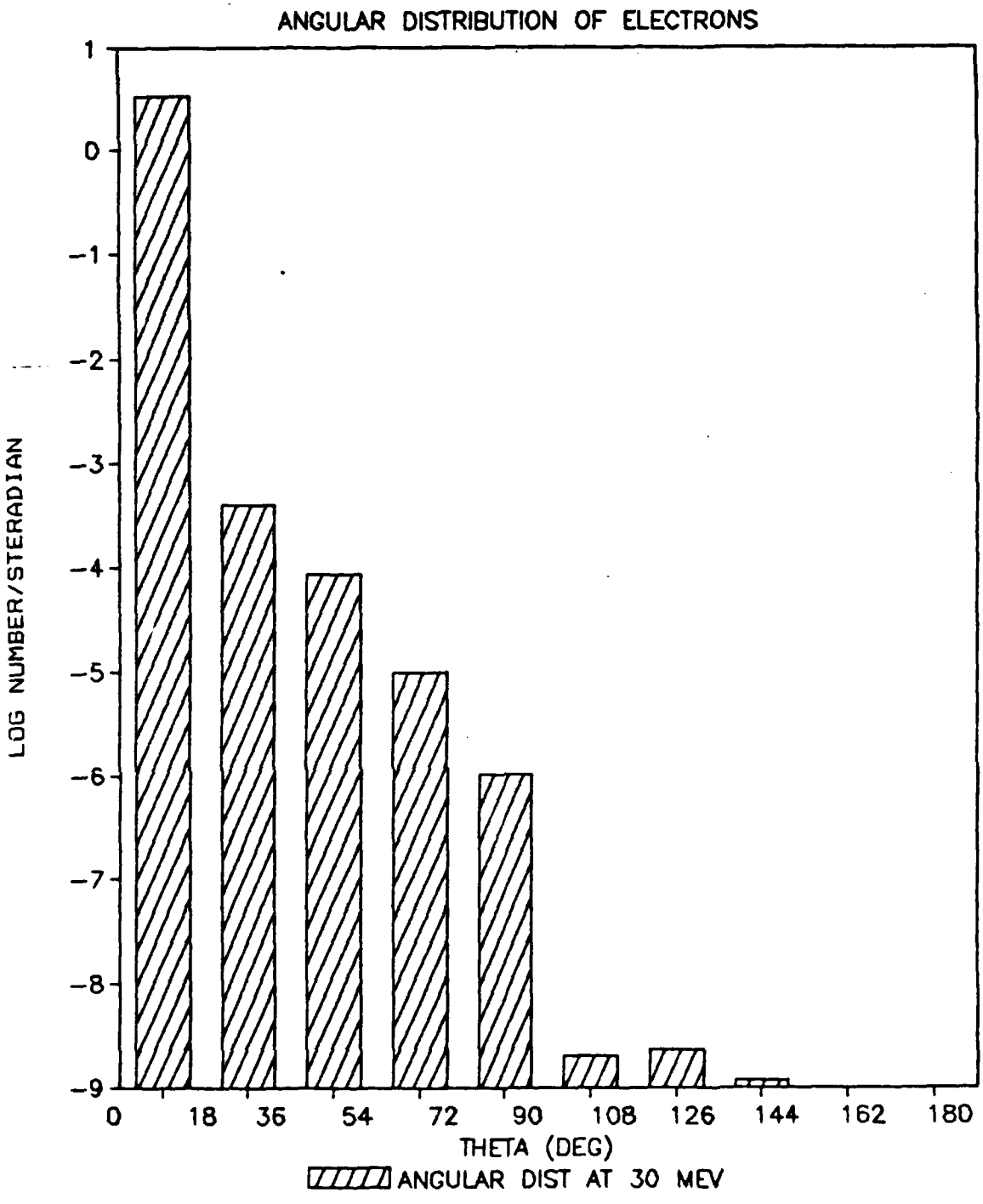


Figure 2-7b. Computer simulation of angular distributions of transmitted and reflected electrons normalized to one incident 30 MeV electron on a 30 mil thick Al_2O_3 target.

collison stopping power (Section B.1.b above) will be used for dose calculations and will be taken to be a constant.

The total energy deposited by n electrons in a thin target of density ρ and thickness d is:

$$E_t = n\, S_{col}\, \rho\, d \quad \text{(MeV)} \tag{2-5}$$

where

$$S_{col} = \frac{dE}{\rho dX}\bigg|_{col}$$

Dividing both sides of Equation 2-5 by the volume gives the total energy deposited into a volume of area A and thickness d.

$$\frac{E_t}{V} = \frac{n}{A}\, S_{col}\, \frac{d}{d}\, \rho \tag{2-6a}$$

This can be written in terms of Φ, the electron fluence in electrons/cm^2.

$$\frac{E_t}{V} = \Phi\, S_{col}\, \rho \tag{2-6b}$$

Dividing through Equation 2-6b by the density gives the energy deposited per gram. Now, by converting the energy from MeV's to ergs, the dose is [Ref. 11]:

$$\text{DOSE} = 1.6 \times 10^{-8}\, \Phi\, S_{col} \text{ Rads (material)} \tag{2-7}$$

$\Phi \equiv$ electrons/cm^2

Equation 2-7 will be used to compute the dose measured in Rads (Si). As previously stated, S_{col} = 1.809 MeV-cm²/g for 30 MeV electrons in silicon.

C. RADIATION EFFECTS ON IGFETs

IGFET devices are majority carrier devices and are therefore relatively insensitive to minority carrier lifetime. This means that they are inherently hard to neutron irradiation. Neutron irradiation will not adversely affect IGFET characteristics until carrier removal is initiated, which occurs at neutron levels of approximately $1X10^{15}$ neutrons/cm² [Ref. 15]. IGFET devices, however, are quite sensitive to total dose of ionizing radiation, which affects the gate dielectric and the field region in bulk silicon devices or the gate dielectric and the back channel in the case of SOI or SOS devices. The rest of this chapter describes these effects in detail.

1. Gate Dielectric

The gate dielectric, SiO_2 (see Fig 2-1), is particularly sensitive to total dose because of the positive charge build-up in the oxide [Refs. 16 and 17]. The charge build-up is brought about by the ionizing radiation freeing the atomic electrons which are then rapidly swept out of the oxide, on the order of picoseconds. The "holes", ionized atoms, are not swept out in the same short time span because of the slow mobility in SiO_2 at room temperature [Ref. 18].

The time span for hole removal in SiO_2 is usually on the order of tens of milliseconds for hardened oxides and hundreds of seconds to years for soft oxides . However, the holes do move under the influence of an applied, or self induced, electric field and can become trapped at trapping sites, or defects, in the oxide. Since the holes do move under the influence of an applied field, the magnitude and direction of the applied bias affects where and how much charge is built-up as shown in Figure 2-8. The charge build-up in the oxide induces an electric field in the channel region thereby causing a decrease in the gate voltage required to turn the transistor on. That is, the threshold voltage becomes less positive for n-channel devices and more negative for p-channel devices. The decrease in threshold voltage is therefore a good indicator of the amount of charge build-up in the gate oxide.

At moderate-to-high radiation, however, negatively charged electronic states are generated at the oxide-silicon interface. These states tend to compensate for the positive charge that is trapped in the oxide layer by repelling electrons from the channel region. At very high doses, these interface states are the dominant damage mechanism and result in an increase in the threshold voltage [Ref. 17]. The effect of these competing mechanisms on gate threshold voltage is illustrated in Figure 2-9 for an n-channel device.

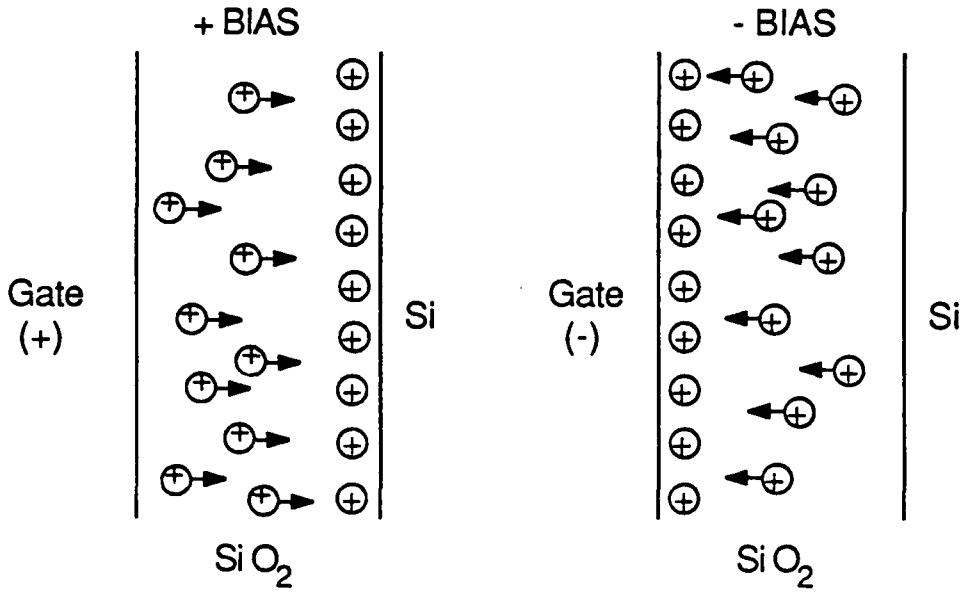


Figure 2-8a Hole migration in SiO_2 under the influence of an applied bias.

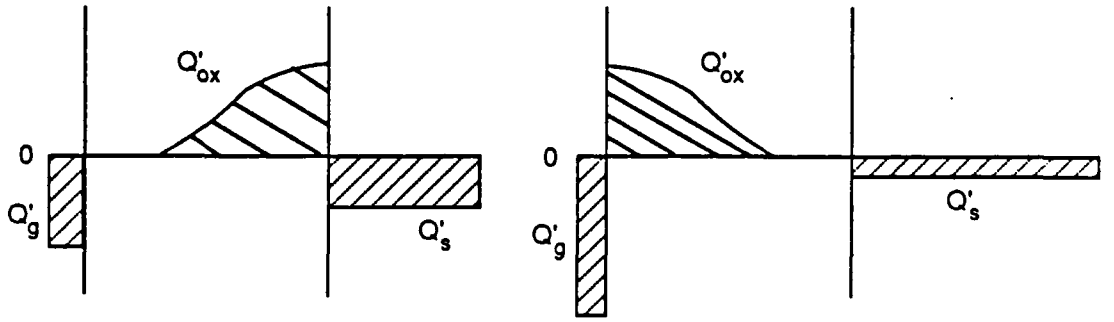


Figure 2-8b Effects of bias on oxide charge build-up at the interfaces. Q'_g = Gate charge per unit area; Q'_{ox} = Oxide charge per unit area; Q'_s = Silicon charge per unit area.

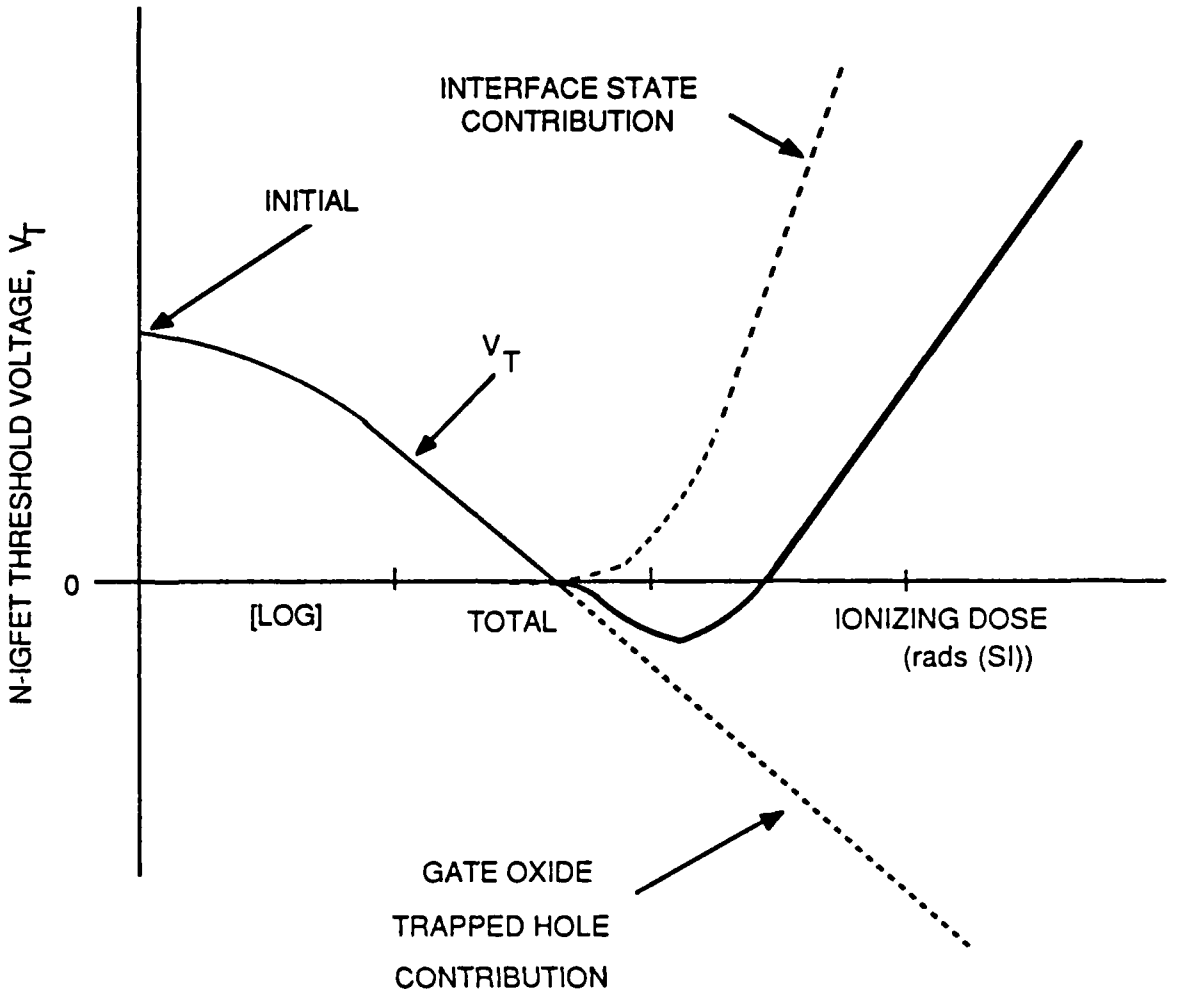


Figure 2-9 N-channel, IGFET threshold voltage shift.

The amount of charge build-up in the gate oxide is proportional to the damage done to the gate oxide. But, even at room temperature, the holes do anneal out over time as they recombine with electrons or cross the oxide-silicon boundary. As the holes in the n-channel device anneal out, the positive charge in the gate oxide decreases, leaving the interface states to determine the threshold voltage shift. The increase in the threshold voltage caused by the interface states may continue to increase the threshold voltage above its pre-radiation value. Annealing of the n-channel IGFET threshold voltage to a value more positive than the initial value is called rebound [Ref. 19].

2. Field Region

The devices used for this thesis are SOS devices and not bulk silicon. The field region inversion is therefore not a problem and will not be addressed. For further information on field oxides, the reader is invited to refer to the appropriate portions of References 10 and 18.

3. Back Channel

The main driving force for the original use of the SOI or SOS paired n- and p-channel IGFETs (commonly called complimentary metal-oxide-semiconductors or CMOS) in military systems was that it offered an absolute fix for the CMOS latch-up problem. However, back channel problems can occur in SOI and SOS technologies.

The original problem of latch-up occurs in CMOS circuits because the normally inactive parasitic bipolar PNP and NPN transistors shown in Figure 2-10 can become forward biased in a gamma-dot environment. The gamma-dot environment generates large photocurrents giving rise to IR drops across the junctions which forward bias the parasitic transistors. Once the junctions are forward biased, the parasitic transistors form a silicon controlled rectifier, SCR, as can be seen in Figure 2-11. If the circuit is not destroyed by the high SCR currents, it still can not return to normal operation until the junctions are no longer forward biased, which normally requires removal of the source voltages, V_D and Vs.

Latch-up can not possibly occur in CMOS circuits employing SOS or SOI technologies because there are no parasitic transistors to become forward biased as can be verified by looking back at Figures 2-2b and c. However, the dose received by the insulator substrate does produce a net charge in the substrate in the same fashion that a net charge is built-up in the gate oxide. The net charge in the insulator substrate can produce a back channel in the silicon between the source and drain along the silicon-insulator interface (Fig. 2-12). This back channel is characterized by an increased leakage current at zero bias which can be in the tens of milliamps range.

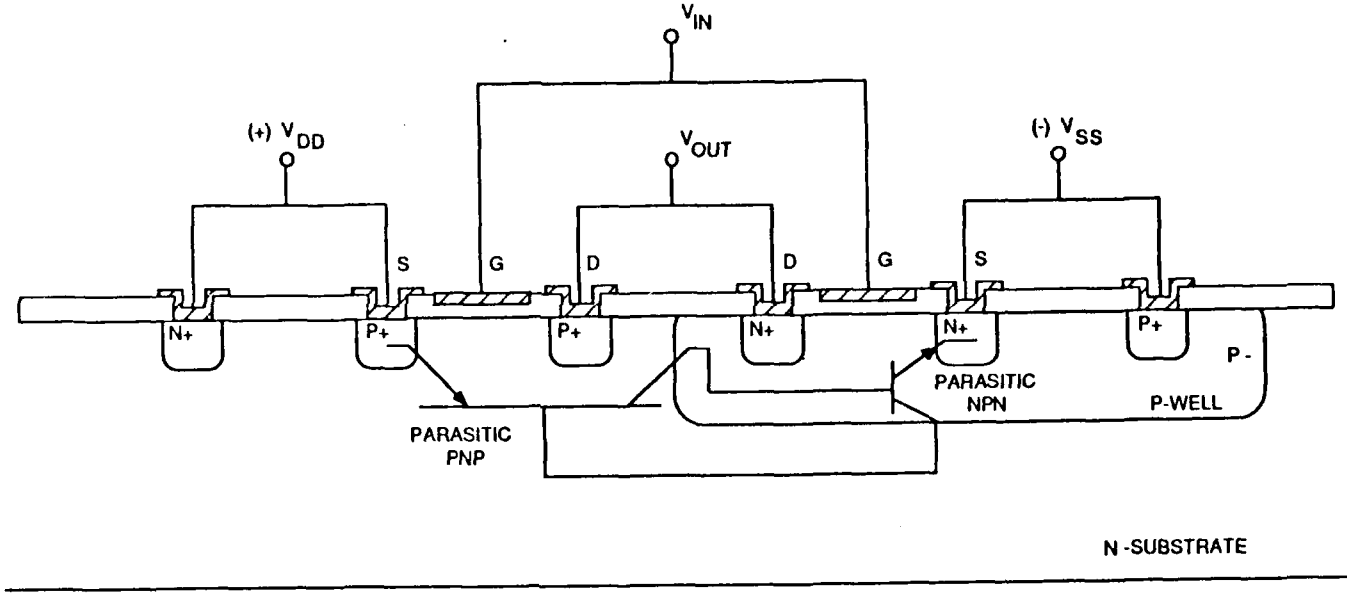


Figure 2-10 Parasitic transistors of a CMOS device.

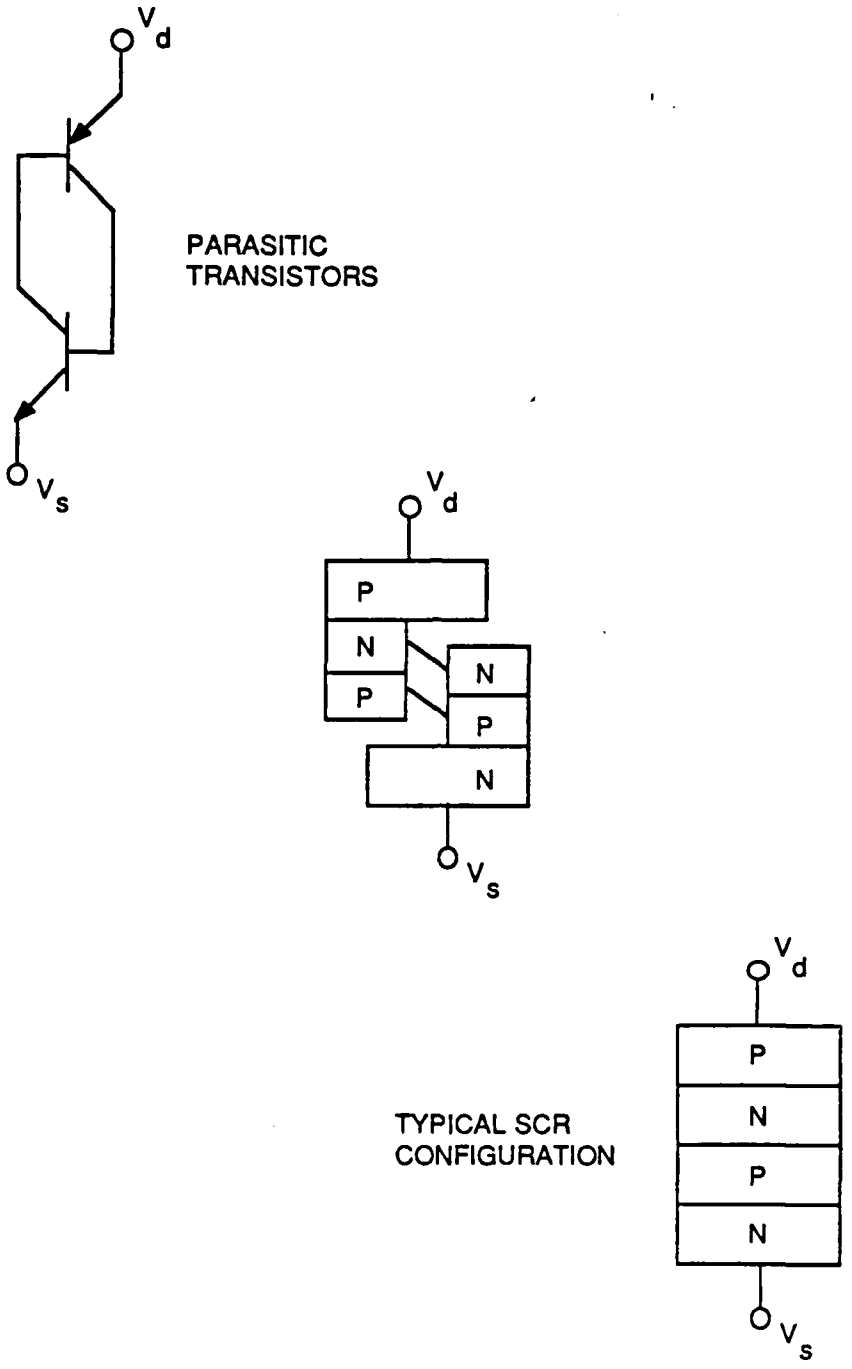


Figure 2-11 The parasatic transistors of the CMOS device form an SCR.

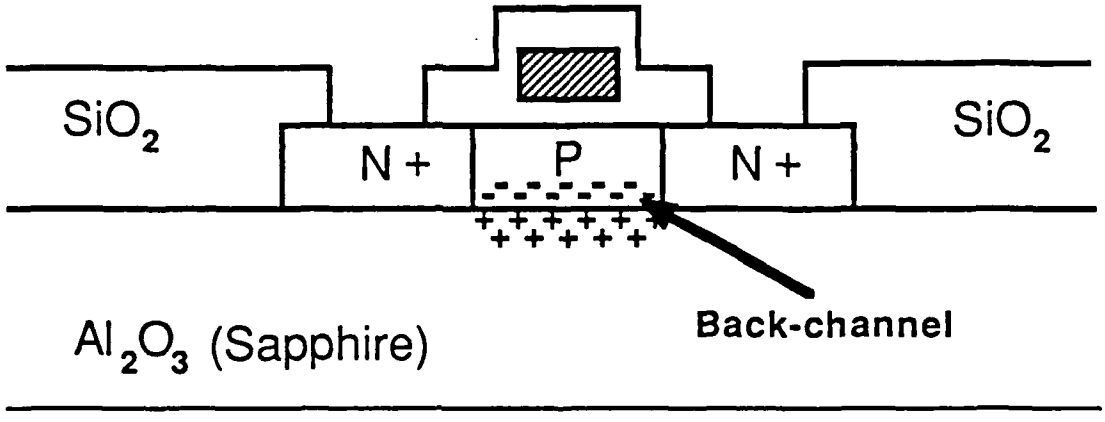


Figure 2-12 Back-channel in SOS IGFET.

III. EXPERIMENT

Research on the SOS devices provided by NOSC was conducted at the Naval Postgraduate School Accelerator Laboratory (NPSAL). The linear accelerator (LINAC) provided 30 MeV electrons used to irradiate the SOS devices which were at ambient temperature (approximately 295 K). The chips were provided in unsealed thirty-four pin flat-packs (Figure 3-1). The chips were intentionally manufactured without metal covers and plastic cases to eliminate the possibility of secondary radiation to the semiconductor chips. The elimination of secondary radiation allowed more precise calculation of the dose received by the devices.

A. DEVICE FABRICATION

The SOS devices were fabricated at NOSC, San Diego, California, on SOS wafers obtained from Union Carbide. The fabrication specifications and procedures (Appendix A) were conceived by Ron Reedy. The fabrication process was conducted at temperatures below 850° C. If the devices are processed at temperatures above 900° C, degradation of the oxide coating reduces the radiation tolerance of the devices [Ref. 6].

Field implantation was done using boron at 30 KeV. The boron concentration was 10^{15} cm $^{-3}$ for the devices used in

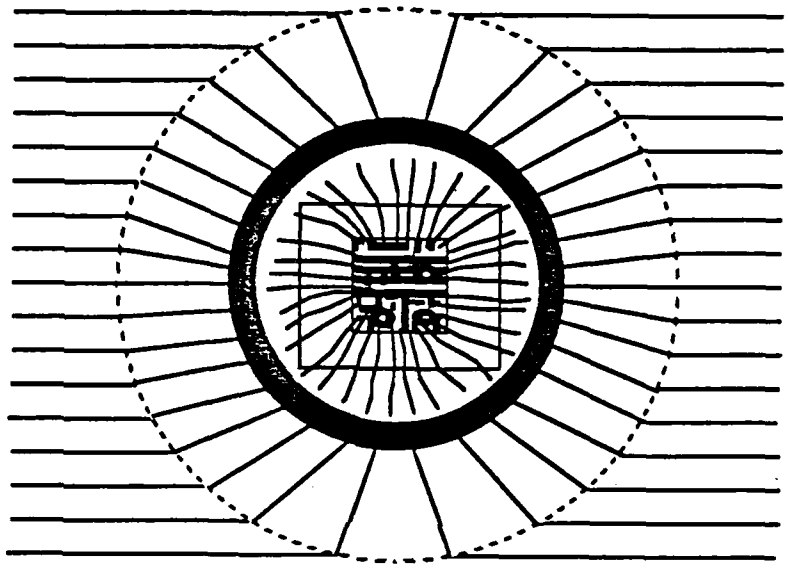


Figure 3-1 SOS IGFET Chip

this thesis. Three gate sizes, 5, 10 and 15 microns, were produced to allow for different device gains (Fig. 3-2).

B. NPSAL LINAC

The LINAC at the Naval Postgraduate School is a traveling wave type patterned after those built at Stanford University in the early 1950's [Ref. 20]. The LINAC is a disk loaded, circular wave-guide, thirty feet long in three ten foot sections (Fig. 3-3). It consists of a series of three klystrons used to accelerate electrons to relativistic energies of from 15 MeV to 100 MeV. The experiments on the SOS devices were conducted using 30 MeV electrons which required only one klystron. The LINAC pulses sixty times per second with a pulse duration of approximately one microsecond. Relativistic electrons are focused on a target inside the target chamber (held at a vacuum of 1 μtorr) with quadropole magnets. The beam area is variable from a one millimeter diameter spot to a few square centimeter rectangle. A one square centimeter square was obtained before each irradiation of a sample by focusing the beam on the phosphor screen described in Section C.1. of this chapter. The centimeter square beam was used for the SOS device irradiation.

Electron fluence is measured utilizing a secondary emission monitor (SEM) located inside the target chamber. As electrons strike the SEM, a capacitor is charged and the

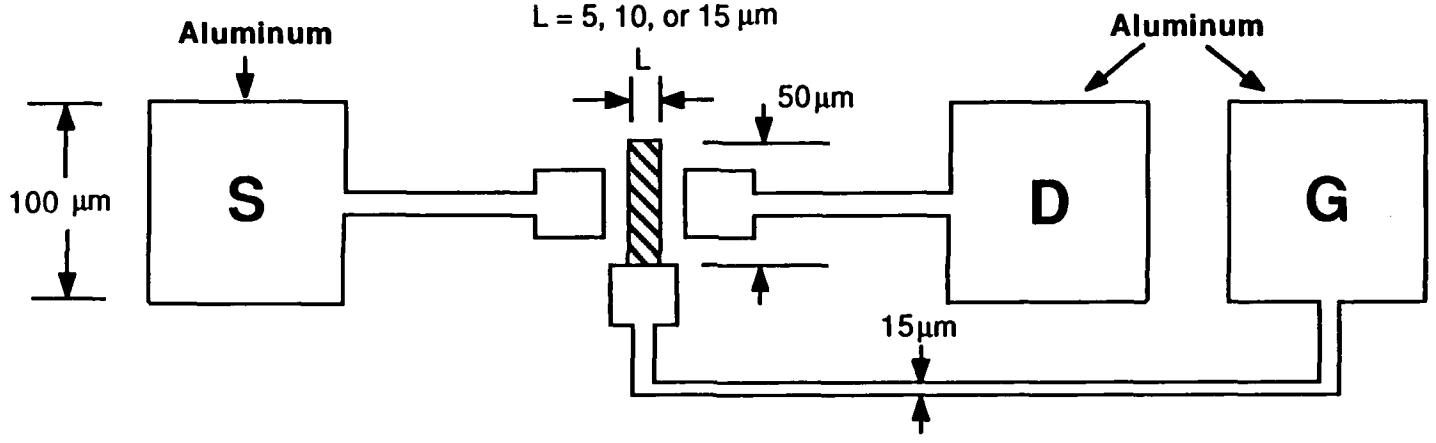


Figure 3-2 Device Layout. Metalization mask and polysilicon gate (Cross-hatched area).

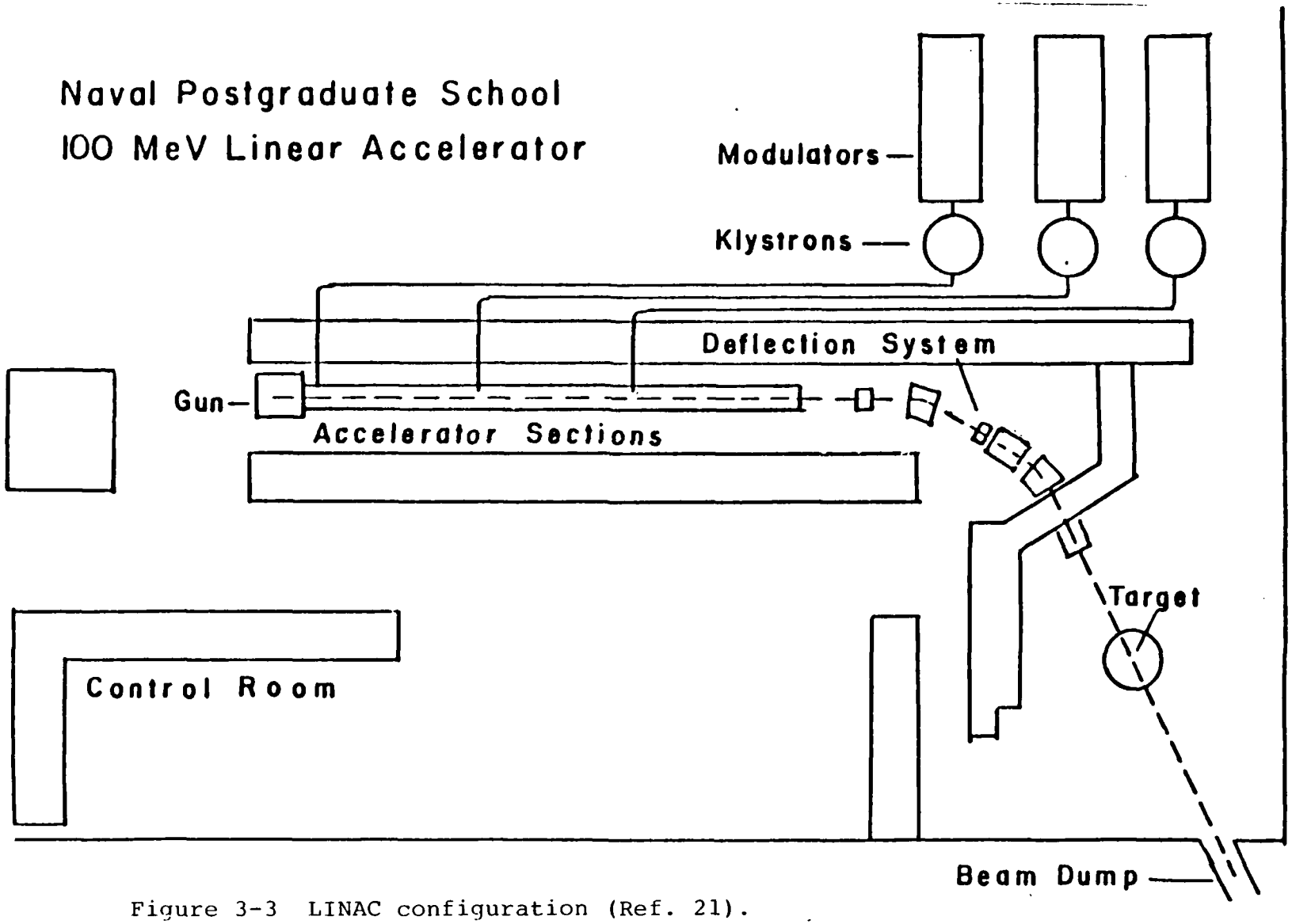


Figure 3-3 LINAC configuration (Ref. 21).

voltage is measured across the capacitor using a voltage integrator circuit. The total number of electrons that have passed through the SEM is determined by:

$$N = Q_B/q \qquad (3-1)$$

where N is the total number of electrons, q is the charge per electron and Q_B is the beam charge.

Previous scattering experiments used a Faraday cup to calibrate the large SEM. The electron collection efficiency of the large SEM was determined to be 6% [Ref. 22]. The Faraday cup has since been removed and the large SEM has become the standard for electron beam fluence. The small SEM used in this thesis was calibrated against the large SEM and determined to be 2.6% efficient at collecting electrons. Using this information and the general charge relationship for a capacitor:

$$Q = C\ V \qquad (3-2)$$

where Q is the charge, C is the capacitance and V is the accumulated voltage, Equation 3-1 becomes:

$$N = C\ V/(0.026\ q) \qquad (3-3)$$

By dividing both sides of Equation 3-3 by the beam area, A, the fluence is determined to be:

$$\Phi \equiv \text{Fluence} = C\ V/(0.026\ q\ A) \qquad (3-4)$$

C. EQUIPMENT SET-UP

1. Chip Mounting

Each semiconductor chip package was mounted on a target chamber test stand. The stand utilized a fabricated flat-pack mount for external connections to the individual devices on the chip. The external connections allowed the voltages of individual chip devices to be varied. A phosphor coated target foil with one-half centimeter reference grid lines was attached directly below the flat-pack mount (Fig. 3-4). The phosphor glowed when subjected to electron beam bombardment. The bright phosphor spot allowed focusing of the electron beam before moving the chip into the beam. O'Reilly [Ref. 23] has determined that the beam spot size shown on the television monitor is 25 per cent larger than the actual beam area for a new phosphor screen. The error decreases to zero as the phosphor screen is "seasoned" in the beam. The beam area was corrected for this known error.

2. Test Equipment Hook-Up

The list of test equipment used in the experiment is contained in Appendix B. Specific comments on equipment usage and limitations will be presented when applicable. Three tests were performed to obtain the data required for determination of device operating characteristics.

The equipment hook-up for obtaining threshold voltage and transconductance data is shown in Figure 3-5.

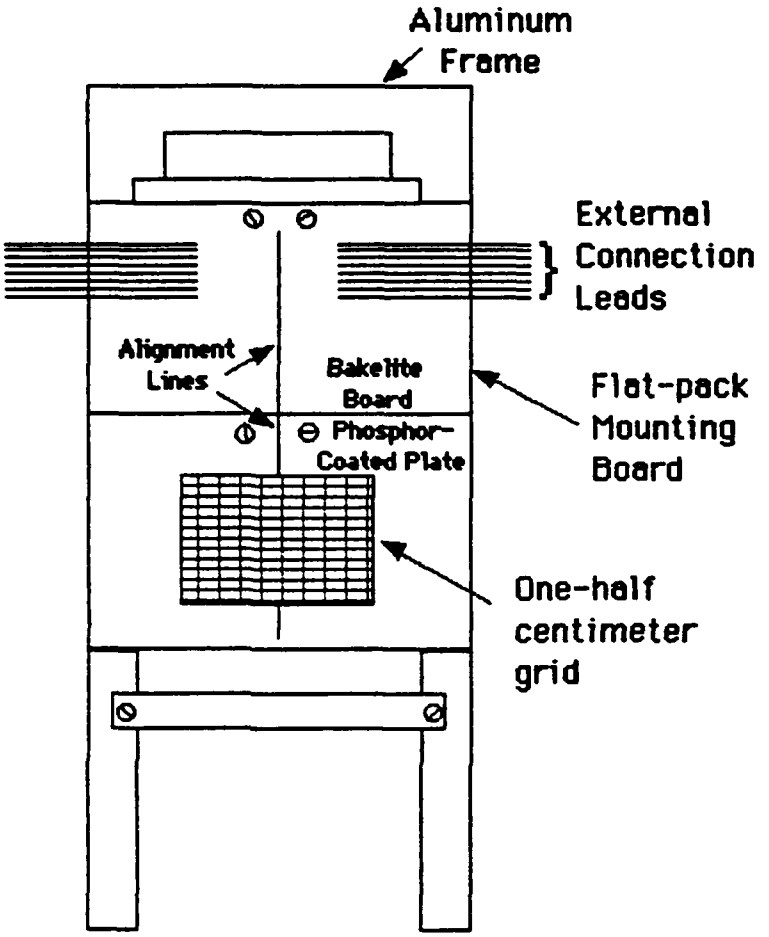


Figure 3-4 Target chamber test stand.

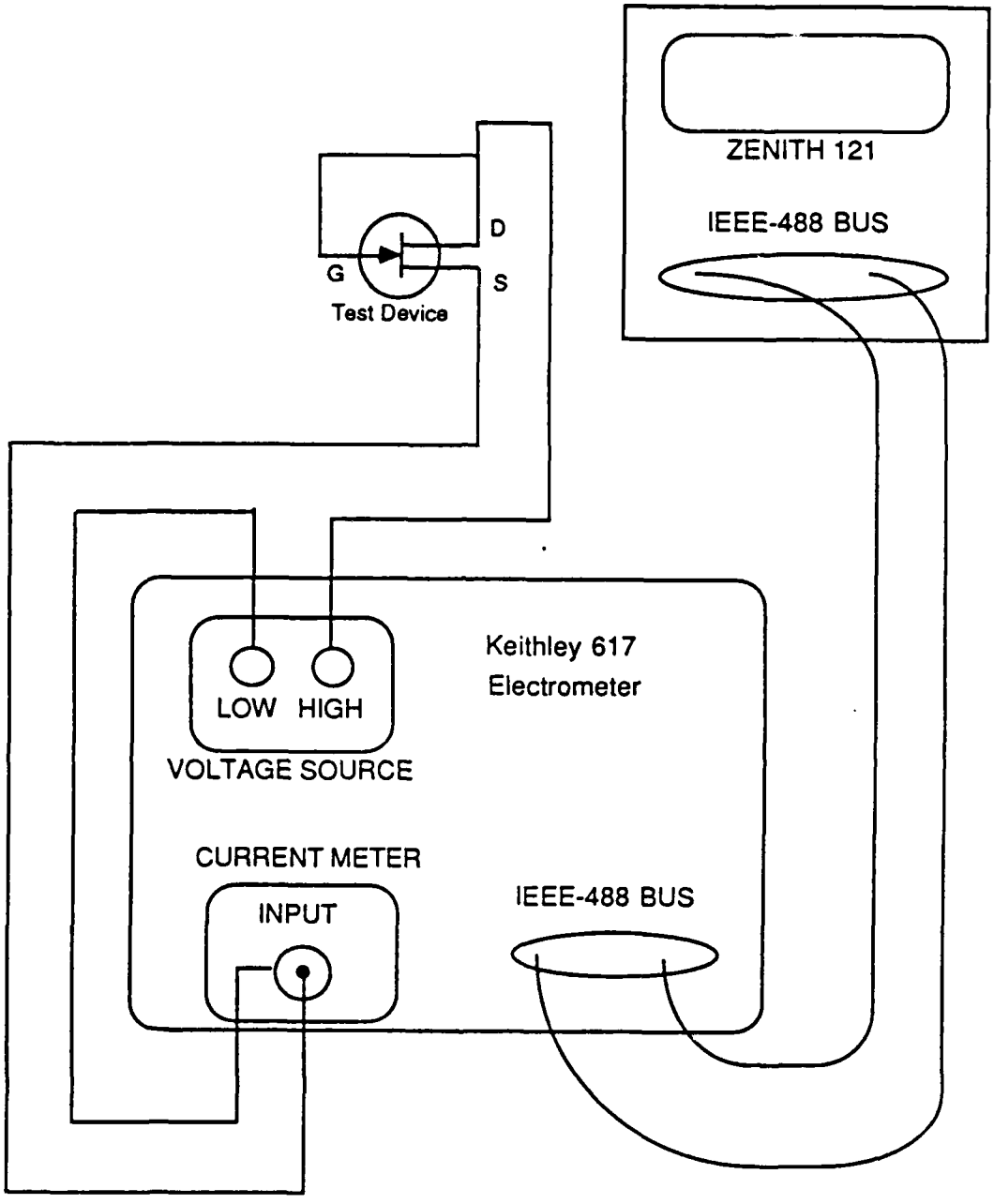


Figure 3-5 Test equipment set-up for transconductance and threshold voltage data.

The technique of tying the drain and gate together (described in Chapter II) was employed in this test set-up. The Keithley 617 was used as the voltage source and electrometer. The 3.6 milliamp current limit of the voltage source caused some limiting of the collected data for the bulk silicon devices used for comparison purposes. The current limit was not considered a serious limitation since the maximum allowable bulk silicon device current was 5 milliamps. The current limitation of the voltage source did not effect the SOS device data collection since all current readings were below 0.3 milliamps.

A Basic language computer program (Appendix C) was written to interface the Zenith 121 computer and Keithley test equipment via an IEEE-488 interface bus. The computer's speed for repetitive operations was used to obtain the numerous voltage versus current data points required for the threshold voltage and transconductance data. A graphic display of the recorded data is shown in Figure 3-6. The data of all four devices on a single chip could be collected within twelve minutes of the completion of irradiation. This was done to minimize the post-irradiation annealing of the damage received by the devices. More importantly, this process ensured that all devices had annealed for the same period of time prior to taking data, giving consistency to the data readings.

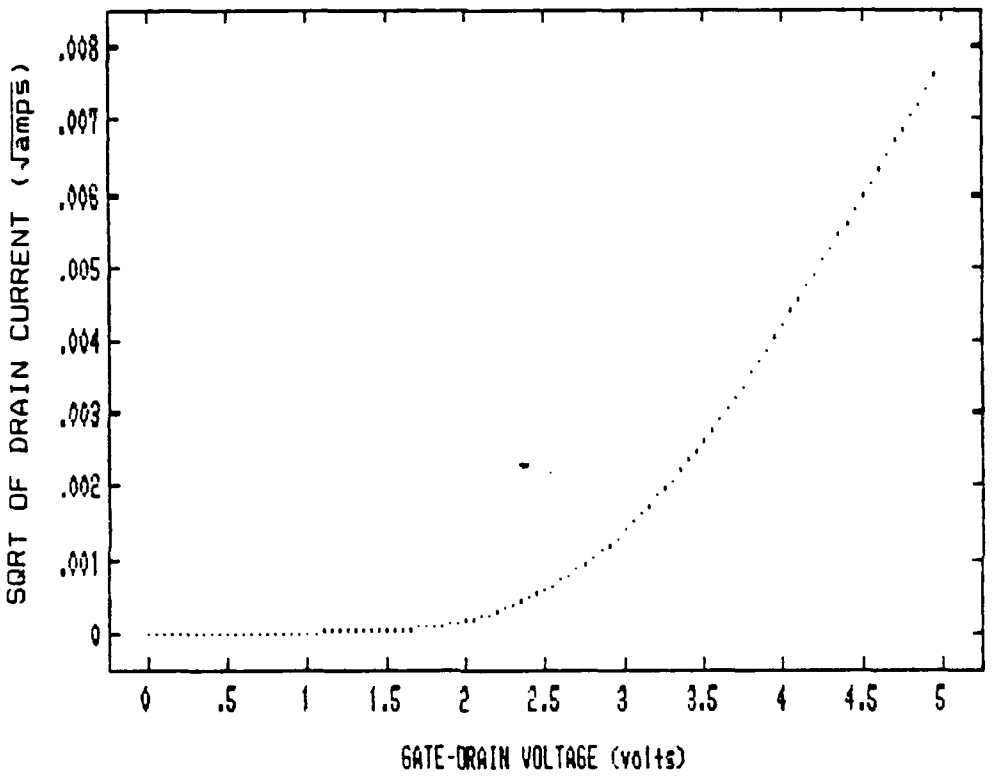


Figure 3-6 Representative graph of the data used for determining g_{max} and V_T. The graphs used for determining all the data points are contained in Appendix D.

The second equipment set-up (Fig. 3-7) was used to obtain leakage current readings at low drain-to-source voltages for the bulk silicon devices. The computerized collection of data for this test was completed using the same computer program written for the SOS data collection process. Leakage current readings for the SOS devices were taken using the previously described equipment set-up for threshold voltage and transconductance data. It was possible to use this same set-up because the current was constant for applied voltages from zero to one volt.

The data obtained by the computer fit the requirements of a square law device (see Eq. 2-1). However, it was necessary to ascertain that the square law device was indeed a transistor. The curve tracer confirmed the operation of the test device to be a transistor.

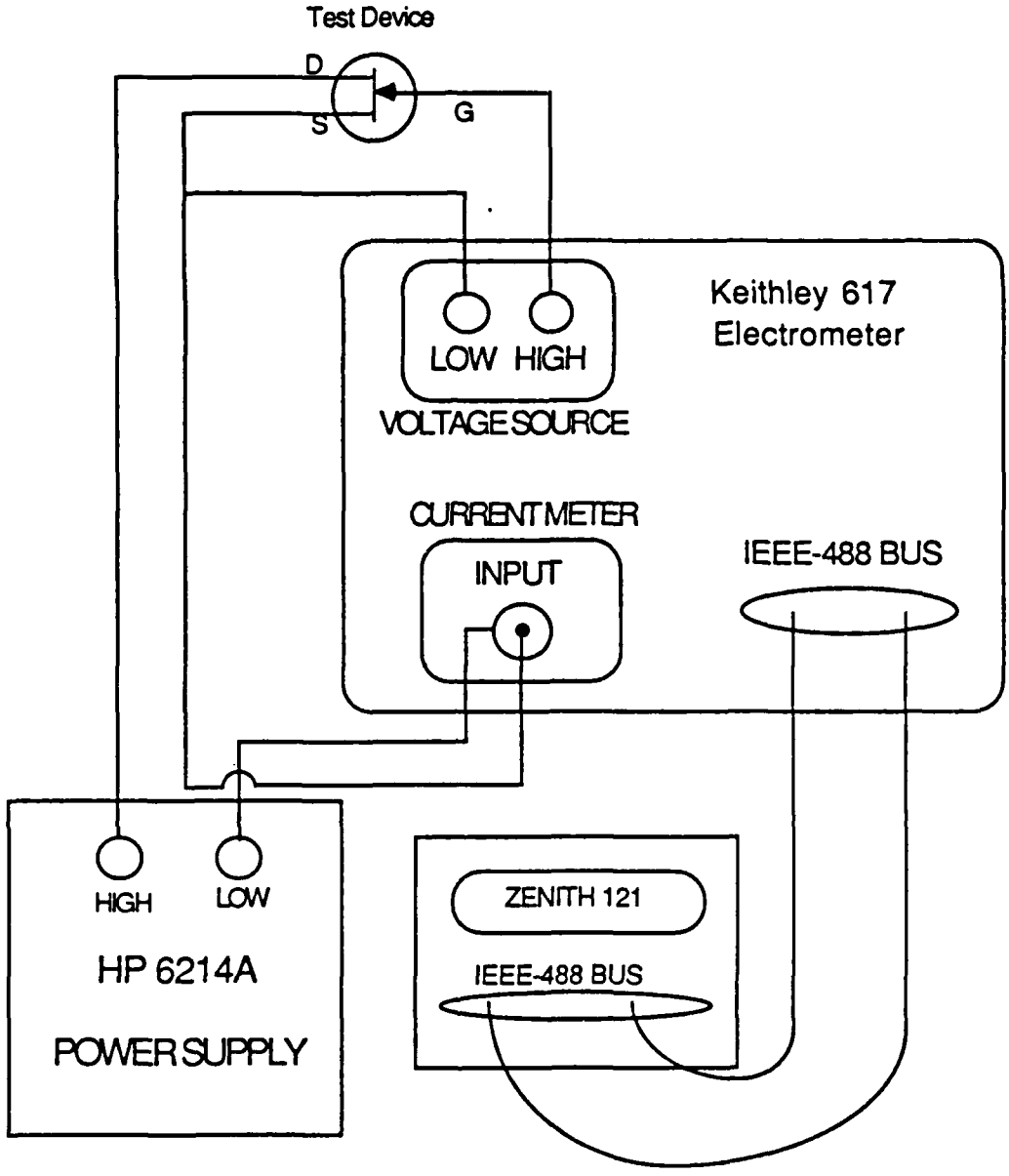


Figure 3-7 Test equipment set-up for leakage current data.

IV. DATA AND ANALYSIS

In the experiment completed, nine SOS IGFETs on three different chips were irradiated with 30 MeV electrons at doses from 10^4 Rads (Si) to 10^6 Rads (Si). The three SOS chips were labeled M, L and S with the devices on each chip labeled A, B, C and D. Out of the twelve possible devices on the three chips, only nine were operational. Drain current versus gate voltage data was taken before and after each irradiation for these nine devices as outlined in Chapter III. Threshold voltage and g_{max} were obtained from plots of this raw data (Appendix D). The data is analyzed in this chapter and discussed in Chapter V.

A. THRESHOLD VOLTAGE DATA

Threshold voltage data was obtained as follows. The devices were exposed to increasing dose levels. The first dose that a device was exposed to was recorded. The next time the same device was exposed, the dose level was an order of magnitude greater. Each successive exposure of the same device was approximately an order of magnitude greater than the previous dose. This procedure minimized the effects of the previous exposure on device response. Tables 4-1 and 4-2 give the individual doses and the total accumulated doses for the samples.

TABLE 4-1
DOSES FOR CHIP M

	Individual Dose (Rads (Si))	Accumulated Dose (Rads (Si))
First Dose	1.0×10^{4}	1.0×10^{4}
Second Dose	1.0×10^{5}	1.1×10^{5}
Third Dose	1.0×10^{6}	1.1×10^{6}

TABLE 4-2
DOSES FOR CHIPS S AND L

	Individual Dose (Rads (Si))	Accumulated Dose (Rads (Si))
First Dose	1.0×10^{4}	1.0×10^{4}
Second Dose	1.0×10^{5}	1.1×10^{5}
Third Dose	5.2×10^{5}	6.3×10^{5}
Fourth Dose	1.0×10^{6}	1.6×10^{6}

I_D versus Vg was measured before and after each dose. The square root of I_D versus Vg was plotted from this data (Appendix D). The threshold voltages listed in Table 4-3 were obtained using the method outlined in Chapter II (see Fig. 2-4). Since threshold voltages vary from device to device, all threshold voltages were normalized to one to aid in comparison of the data on a single graph. Normalization was accomplished by dividing the threshold voltage by its

TABLE 4-3
THRESHOLD VOLTAGE IN VOLTS

Gate Size (microns)	10	5	10	15	5	5	15	15	5
Dose (Rads (Si))	Chip and device identifier MA	MB	MC	MD	SB	SD	LB	LC	LD
Pre-Rad	3.38	3.18	1.95	3.30	2.80	2.78	2.55	2.60	2.75
1.0×10^{4}	3.05	2.86	1.55	1.45	2.68	2.60	2.48	2.65	2.66
1.1×10^{5}	2.25	2.13	0.78	2.60	1.25	1.65	1.70	2.25	1.66
6.3×10^{5}					0.35	0.50	0.65	1.05	0.68
1.1×10^{6}	0.13	0.50	-0.5	0.83					
1.6×10^{6}					0.25	0.13	0.00	0.40	0.40
Hours after Final Irradiation									
19						1.50			
27							1.88	1.70	1.71
59							2.15	1.85	2.00
83	2.25	2.48							
107	2.25	2.55							

pre-irradiation value. Figure 4-1 shows the plot of normalized threshold voltage versus total dose. The threshold voltages decreased rapidly with increasing dose above 10^4 Rads (Si).

The samples underwent annealing at room temperature. The annealing affects upon threshold voltage are shown in Figure 4-2. Three devices, one-third of the total tested, failed during the annealing period. Two of these devices failed due to mechanical damage. The damage would not have occured if the chips had been packaged for actual circuit usage. As previously stated, the chips were packaged for experimental work and extremely susceptible to failure from mechanical shock. The mechanical shock could be as small as a breeze or a piece of paper. Forces as small as these can cause dislodging of the thin bonding pad wires. The third device failed for unknown reasons.

B. GAIN DATA

The saturation transconductance, $g_{m(sat)}$ (Eq. 2-2b), is listed in Table 4-3 for each total dose and annealing time. The normalized transconductance versus dose and annealing time are plotted in Figures 4-3 and 4-4, respectively.

C. LEAKAGE CURRENT

No significant data was obtained for leakage current. The reasons for this and a possible method for obtaining useful data will be discussed in Chapter V.

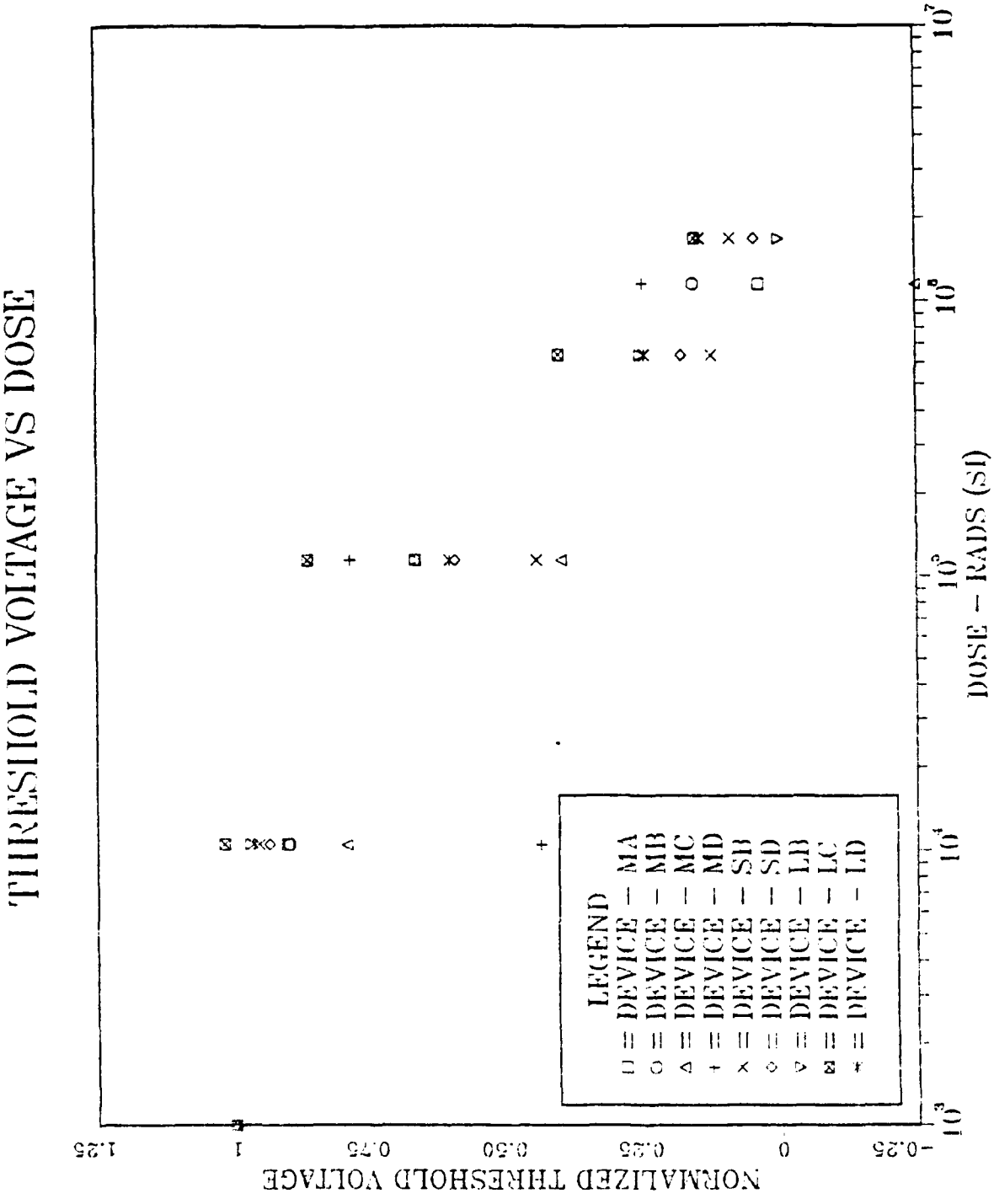


Figure 4-1 Normalized threshold voltage versus dose.

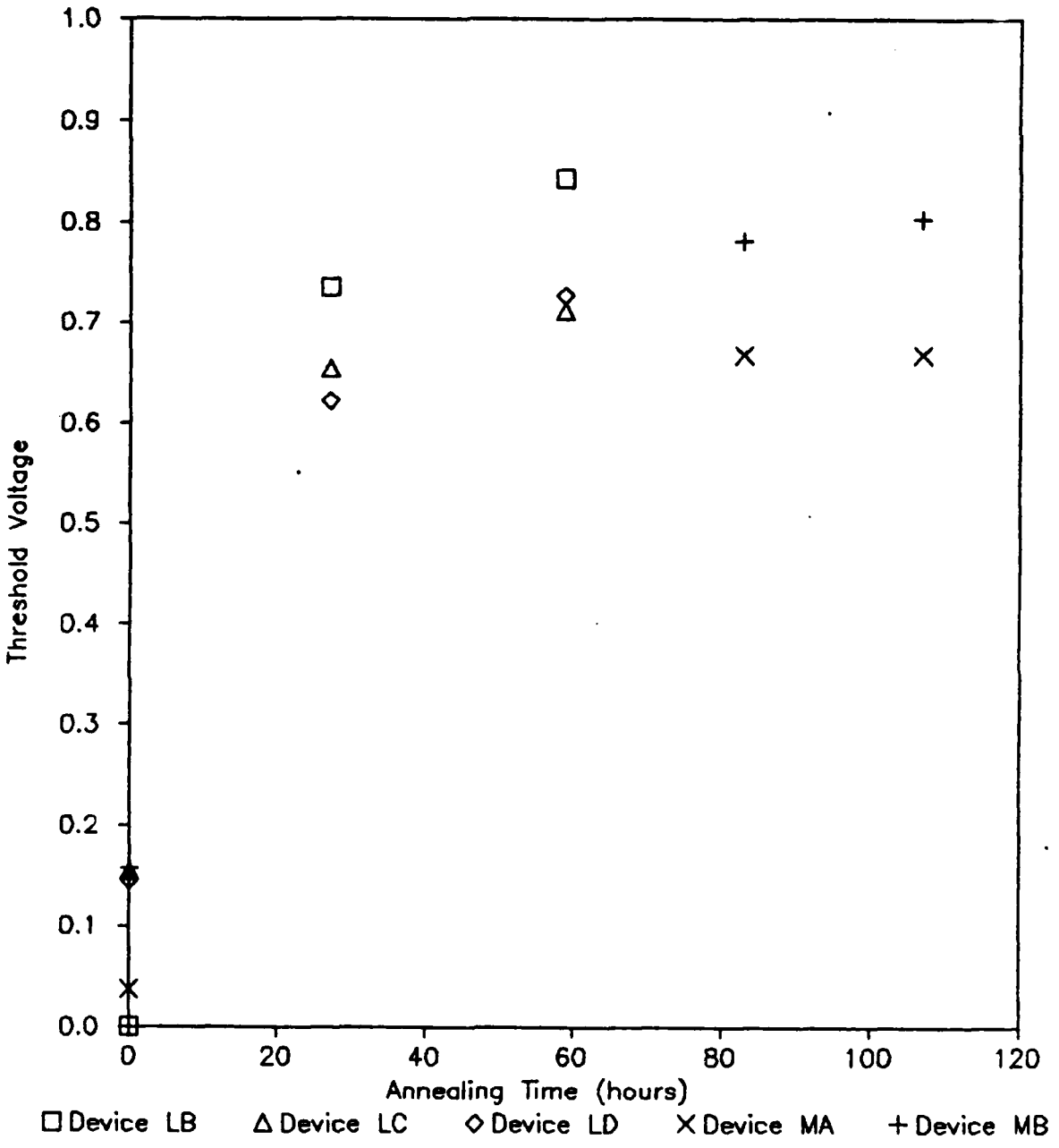


Figure 4-2 Normalized threshold voltage versus annealing time.

TABLE 4-4
SATURATION TRANSCONDUCTANCE IN MICROMHOS

Gate Size (microns)	10	5	10	15	5	5	15	15	5
Dose (Rads (Si))	Chip and device identifier MA	MB	MC	MD	SB	SD	LB	LC	LD
Pre-Rad	4.63	8.48	6.14	4.42	12.53	12.01	3.31	3.09	10.42
1.0×10^4	5.08	8.70	6.40	5.96	13.72	12.47	3.86	3.43	11.40
1.1×10^5	6.86	10.23	7.42	5.75	11.40	13.93	4.36	4.96	9.72
6.3×10^5					9.40	13.03	4.21	4.11	9.74
1.1×10^6	3.56	5.59	5.84	3.04					
1.6×10^6					8.17	11.85	3.03	3.10	8.53
Hours after Final Irradiation									
19						10.43			
27							2.49	2.17	6.63
59							2.20	1.96	6.31
83	3.04	5.36							
107	2.91	5.58							

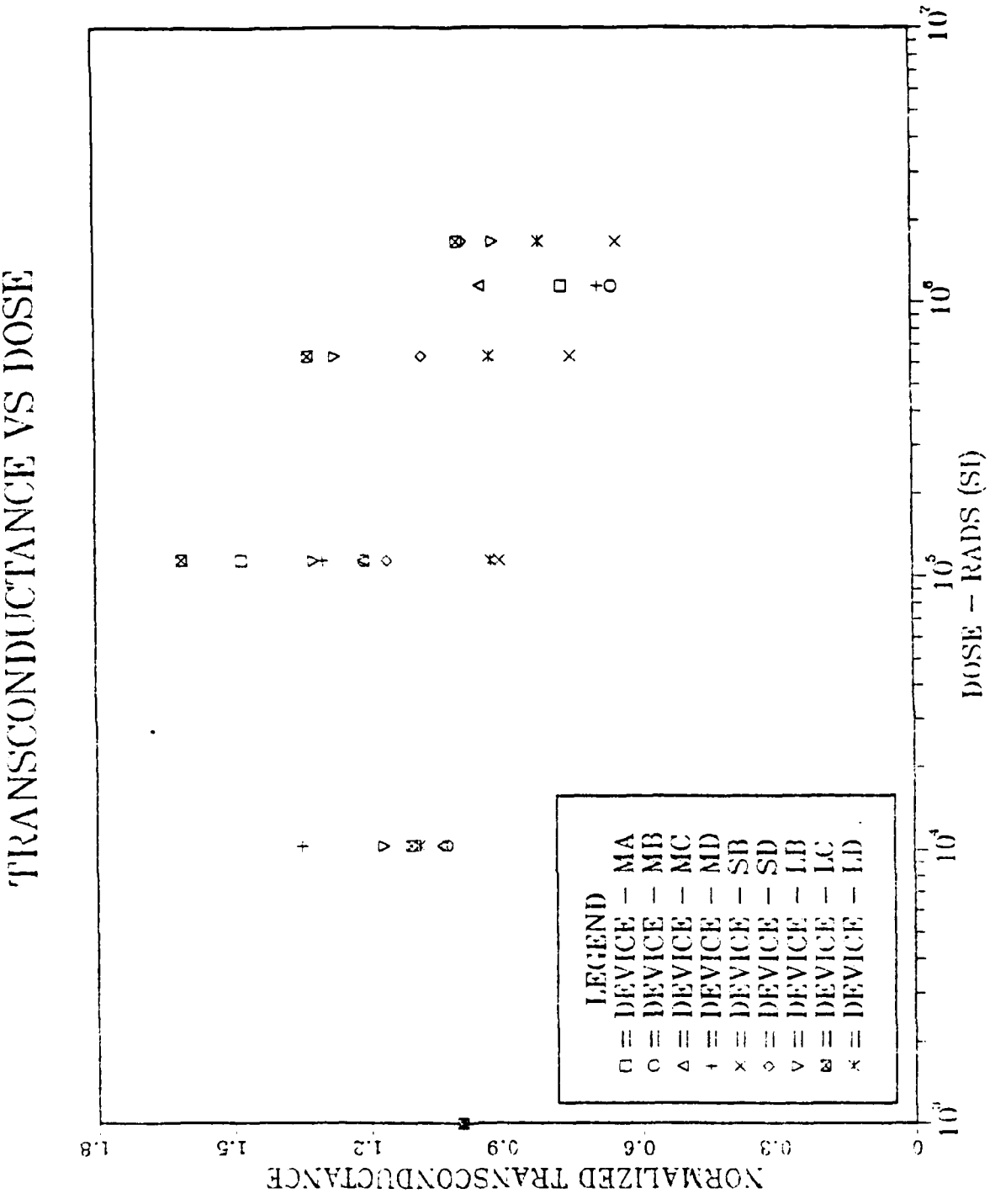


Figure 4-3 Normalized transconductance versus dose.

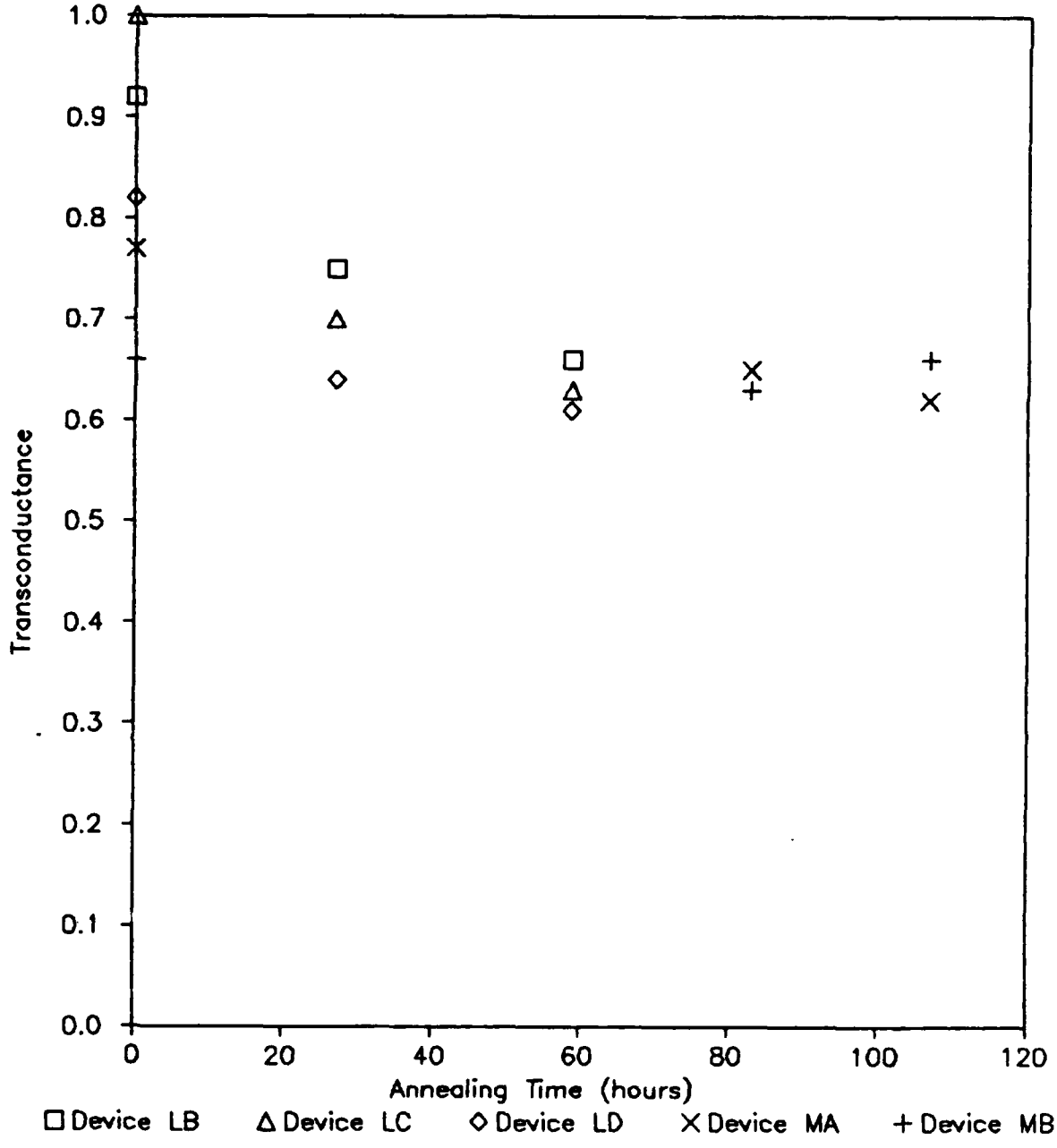


Figure 4-4 Normalized transconductance versus annealing time.

V. DISCUSSION AND CONCLUSIONS

A. DISCUSSION

1. Threshold Voltage

The threshold voltage decreased with increasing dose (see Fig. 4-1). The shape of the curve was in agreement with that expected for the gate oxide trapped hole contribution (see Fig. 2-9). The portion of the curve labeled interface state contribution was not observed. This portion of the curve might have become apparent, if the total dose were increased to 10^{8} or 10^{9} Rads (Si).

Threshold voltage is affected by annealing at room temperature. A plot of threshold voltage versus time is shown in Figure 4-2. Rapid annealing should occur during the period of high oxide charge concentration. Since the affects of annealing on threshold voltage slowed after twenty four hours, it appears that a large percentage of charge dissappeared during this period.

2. Transconductance

Saturation transconductance, $g_{m_{sat}}$, was the circuit gain parameter. It was used to determine the effects of radiation on the product of mobility and capacitance per unit area, μC_{ox} (Eq. 2-2b). $g_{m_{sat}}$ increased initially and then decreased with increasing dose (Fig. 4-3). $g_{m_{sat}}$ continued to decrease during the entire annealing period (Fig. 4-4).

The initial increase in g_{max} (Fig. 4-3) indicates an increase in μ, C_{ox} or both. The decrease in g_{max} as dose increased was expected. The increased charge and defect density after irradiation would increase the carrier collision rate and decrease carrier mobility [Refs. 6 and 10].

3. Leakage Current

The lack of useful leakage current data was caused by an incorrect measurement procedure (Chap. III). An attempt to measure the leakage current with a small drain to source voltage was not successful. This method did not detect the changes in leakage current, caused by a back channel leakage path.

Reference 4 explains a test set-up procedure to measure leakage current. The drain to source voltage should be set to 5 volts and the gate should be grounded. The drain current can then be monitored for leakage current. The relatively large drain to source voltage will produce a back channel leakage current if the back channel exists. The grounded gate should minimize the amount of normal subthreshold-voltage leakage current.

B. CONCLUSIONS

1. Summary

The n-channel IGFET is an integral part of CMOS technology. The n-channel IGFET has a higher current output

capability than the p-channel IGFET. The higher current output is due to the greater mobility of electrons as the majority carrier [Ref. 10]. The characteristics of the n-channel IGFET make it an important device for electronic circuit construction.

The threshold voltage reached fifty percent of its pre-irradiation value at 10^{5} Rads (Si) but the n-channel SOS IGFETs tested were operational to a total dose of 10^{6} Rads (Si). This total dose level is at the forefront of SOS technology [Ref 8]. Decreasing the gate thickness should improve the IGFET's radiation hardness beyond its present value [Ref. 6].

The device gain decreases somewhat during irradiation (Fig. 4-3) and continues to decrease during the annealing period (Fig. 4-4). For some devices tested, the decrease in g_{max} is as high as 50 percent. Dawes [Ref. 6] states that mobility decreases as much as 30 percent at 10^{5} Rads (Si). The decrease in g_{max} could be due to a decrease in mobility (Eq. 2-2b).

Successful back-channel leakage current data was not obtained.

2. Suggestions

A method of measuring C_{ox} directly needs to be developed so mobility can be obtained from the g_{max} data. If the source, gate and drain aluminum contacts have been deposited on the individual SOS devices, they will have to

be taken into consideration when measuring C_{ox}. If the contacts have not been deposited, a method of connecting the test equipment to the devices will have to be devised. Development of a method of measuring C_{ox} will not be easy and, possibly, a method of measuring mobility directly would be easier to develop.

The method of measuring back-channel leakage current discussed in Section A above should also be implemented. Power consumption in integrated circuits is an important consideration and must be kept to a minimum. The effects of an increased leakage current would be an important parameter to monitor.

The experiment should be conducted again when NOSC has developed a thinner gate oxide n-channel IGFET. The results can then be compared to see if radiation hardness has actually increased as predicted.

APPENDIX A

FABRICATION SPECIFICATIONS

This is the run sheet provided by Dr. Ron Reedy of NOSC for the SOS device fabrication.

OVERALL RUN DESCRIPTION
RR-12 PROCESS 303B

This is the run sheet for the B process of the 303 mask set. This run of this process is labelled RR-12. Ron Reedy should be contacted for inspection after completion of each line item. All insertions into furnaces should be done with a 10 minute push and pull time, as the sapphire substrates are susceptible to breakage, especially during pulls from high temperature furnaces.

MATERIAL

There will be four SOS wafers from the Union Carbide lot received in April, 1985 and miscellaneous n and p type test wafers (abbreviated TW with identity number) as noted. The wafers are labelled SOS 60, 61, 62 and 63.

THREE PROCESS SHEETS ARE ATTACHED

PROCESS 303B, CMOS SOS

Date In	Out	Description	Meausrements
		Field implant, B, SOS 60 and 61 75 keV, 5E11 cm-2 and 30 keV, 5E11 cm-2 SOS 62 and 63 75 keV, 1E12 cm-2 and 30 keV, 1E12 cm-2	
		Grow 300 Angst SiO_2, Gate, 20 min., steam 875°C, NO HCl during growth, but SC1&2	
		Deposit 3,000 Angst SiO_2 in ROTOX	
		Densify, 875 °C, photo, NEG resist (303-1), etch SiO_2 ALL IN ONE DAY	
		Etch Si (equal weights KOH and DI H20, cover with n-propyl etch at 70°C CONTINUED ON NEXT SHEET	

PROCESS 303B, PAGE 2

Date In	Out	Description	Meausrements
		Photo (303-2), etch	
		Add p-type TW1 for C-V Grow 925 A gate oxide 55 min., F=8.5, 875°C, steam NO HCl during gate growth Hold TW1 for CV	
		Add TW2 with SiO2 Deposit 3,000 A LPCVD 625 °C, 27 min.	
		Dope n^+, 850 °C, 5-200-5 strip P2O5 Measure ρ of TW2	
		Photo (303-3), except TW2 Doped poly etch then oxide etch	
		Add p type TW3 Dope n^+, 850 °C, 5-200-5 strip P2O5 Measure ρ of TW3 CONTINUED ON NEXT SHEET	

PROCESS 303B, PAGE 3

Date In	Out	Description	Meausrements
		Rotox 5,000 A SiO2 Densify 30 min in deglaze	
		photo (303-4), etch	
		Deposit 8,000 Angst Al,	
		photo (303-5), etch metal	
		Sinter, 450°C, N2+H2	
		GO TO THE HEAD OF THE CLASS	

PHOTO & ETCH DESCRIPTIONS

1. 303-1

Spin 45 CST 747 Neg resist @ 6000 RPM
Soft bake 30 min. @ 75 °C
Expose 4.0 sec @ 80 watts
Dev. 1.0 min.
Hard bake 30 min. @ 135 °C
Etch 4.0 min oxide etch 10:1 @ 24 °C
Strip resist in Sulf-perox, 10 min

2. 303-2

Prebake 30 min @ 135 °C
Spin 60 CST 747 Neg resist @ 6000 RPM
Soft bake 30 min. @ 75 °C
Expose 4.0 sec @ 80 watts
Dev. 1.0 min.
Hard bake 30 min. @ 135 °C
Etch 5.0 min oxide etch 10:1 @ 24 °C
Strip resist in Sulf-perox, 10 min

3. 303-3

Prebake 30 min @ 135 °C
Spin 60 CST 747 Neg resist @ 6000 RPM
Soft bake 30 min. @ 75 °C
Expose 4.0 sec @ 80 watts
Dev. 1.0 min., measure C.D.
Hard bake 30 min. @ 135 °C
Etch min poly etch
Etch min oxide etch
Strip resist in Sulf-perox, 10 min
Measure C.D.

4. 303-4

Same as 303-1

5. 303-5

Prebake 30 min @ 135 °C.
Spin 50% HMDS 10 sec., puddle 20 sec., spin 2000 RPM.
Spin NEG 747 resist 6000 RPM, 20 sec.,
Soft bake 30 min @ 75 °C,
Expose 20 sec @ 40 watts,
Develop and rinse, 1min each, blow dry,

Hard bake 30 min @ 135 °C,
Metal Etch: 80 sec with agitation, rinse, dry, rebake 10 min,
bubble etch to clear,
Strip PR in 712D stripper @ 90 °C, 10 min,
30 min rinse, dry.

6. Doped Poly etch

1090 ml Acetic + 272 ml Nitric + 45 ml HF. Etch at 20-22 °C.

7. Undoped Poly etch

833 ml Nitric + 446 ml DI H20 + 52 ml Ammonium Flouride,
Etch @ 24 °C.
Put bare silicon wafer in etch solution to activate and stabilize.
Agitate during etch but DO NOT break to air during etch.
3000 A should etch in approximately 50 seconds.

APPENDIX B

EQUIPMENT LIST

1. Zenith 121 microcomputer with a Pickles and Trout IEEE-488 interface board installed.
2. Keithley Model 617 Programmable Electrometer.
3. Hewlett-Packard 6214A power supply.
4. Tektronix Type 576 curve tracer (with polaroid camera).
5. SOLA 115 v AC Rectifier/Inverter for AC line noise suppression on the test equipment.
6. Microscope for device observations.

APPENDIX C

BASIC LANGUAGE COMPUTER PROGRAM

This Basic language program is used to collect the current versus voltage data in the experiment. The program interfaces with a machine language program, MICSOFT, provided by Pickles and Trout for the operation of their IEEE-488 interface board.

```
1000 '  ==========================================================
1010 '
1050 '  Control characters (such as line feed and carriage return) can
1060 '  be entered into the TALK and CONTROL strings by preceding the
1070 '  control character with an ESCAPE.  For example, to get the string
1080 '  1234<ESCAPE>$%<RETURN><LINE FEED> you would type
1090 '  1234<ESCAPE><ESCAPE>$%<ESCAPE><RETURN><ESCAPE><LINE FEED><RETURN>.
1100 '
1110 ' ==========================================================
1120 '  Initialization Routines
1130 '
1140 '  The purpose of these routines is to initialize the MICSOFT function
1150 '  addresses and the communication variables.
1160 '
1170 DEF SEG                              :'  point to ZBASIC'S segment
1180 '
1190 '   Calculate highest available memory for machine language routines
1200 '
1210 HIMEM=PEEK(2380)*256 + PEEK(2379) - 1500
1220 CLEAR ,HIMEM                         :'  reserve space for routines
1230 '
1240 '   Calculate address of the SETUP routine
1250 '
1260 SETUP=PEEK(2380)*256 + PEEK(2379) - 1500  'machine language subroutine
1270 BLOAD"MICSOFT.M",SETUP               :' load machine language routines
1280 GOSUB 9070                           :'  load keyin routine
1290 '
1300 '  Set up function call address variables
1310 '
1320 CALL SETUP (CNTL%, CNTLC% ,TALK%, TALKC%, LSTN%, LSTNC%, SPOLL%, PPOLL%,
       DREN%, REN%, STATUS%, IFC%, BRSET%, IOSET%, PROTCL%, ECHO%, IOPORT%)
1330 '
1340 '  Call the setup routines to let MICSOFT know what variables to use
1350 '
1360 CLS
1370 CALL IOSET% (ERCODE%, TIM%, POLL%, BUS%)
1380 CALL PROTCL% (EOT%, EOS%, LENGTH%)
1390 CALL ECHO% (ECHOIN%, ECHOOUT%)
1400 '
1410 ' ==========================================================
```

```
1420 '              Device Initialization Routine
1430 ' Initialize addresses and equipment on the 488 bus.
1440 ERCODE%=0
1450 DEVLA$=";"
1460 DEVTA$="["
1470 UNLI$="?"
1480 UNTA$="_"
1490 CNTT$=CHR$(20)
1500 GGET$=CHR$(8)
1510 CALL IFC%
1520 CALL REN%
1530 CALL CNTL%(CNTT$)
1540 A1$="C1XZ1XZ0X"
1550 CALL CNTL%(DEVLA$)
1560 CALL TALK%(A1$)
1570 CALL CNTL%(UNLI$)
1580 CLS :ERCODE%=0
1590 GOSUB 8010
1600 PRINT "Available Routines"
1610 PRINT "1. Diode Curves (decade, constant current from 1nA to 100 microA)"
1620 PRINT "   WARNING: Forward bias direction Only!"
1630 PRINT "            Voltages as high as 300V may be present."
1640 PRINT "2. Voltage vs Current (Reverse or forward bias, 2mA max.)"
1650 PRINT "3. End program."
1660 PRINT "Which would you like to do?     ";STRING$(4,CHR$(8));:INPUT " ",F%
1670 IF F%<1 OR F%>3 THEN 1580
1680 IF F%=3 THEN CLS:END
1690 ON F% GOSUB 2040,2370
1700 GOTO 1580
1710 '
1720 '=============================================================================
1730 '                  DISK INITIALIZATION SUBROUTINE
1740 INPUT "Enter the data file name (include drive and extension) ",NODF$
1750 PRINT "All numbers must be preceeded by a letter. (Example: the date must"
1760 PRINT "not be entered as 7/28/85, but can be entered as D_7/28/85.)"
1770 INPUT "Date of the run ",FDATE$
1780 INPUT "Run number (e.g. R1 or RUN1)",FRUN$
1790 INPUT "SEM voltage obtained ",SEMV$
1800 INPUT "SEM capacitor used (e.g. C_1microfarad) ",SEMC$
1810 INPUT "Beam area (BA1.5 SQ CM) ",BEAMA$
1820 INPUT "Any general comments ",GENCOM$
1830 OPEN "O",#1,NODF$
1840 PRINT #1,"DATE"+FDATE$
1850 PRINT #1,"Run number"+FRUN$
1860 PRINT #1,"SEM voltage"+SEMV$
1870 PRINT #1,"SEM capacitor"+SEMC$
1880 PRINT #1,"Beam area"+BEAMA$
1890 PRINT #1,"General comments: "+GENCOM$
1900 A1$="            Log      Sqrt              Log    "
1910 B1$=" Current  Current  Current  Voltage  Voltage  "
1920 PRINT #1,A1$ :PRINT #1,B1$
1930 RETURN
```

```
1940 '
1950 '=============================================================================
1960 '                    STRIP READING SUBROUTINE
1970 CHK$=LEFT$(A1$,1)                  :'obtain left data byte
1980 IF CHK$="0"THEN 2020               :'and check for normal or overflow
1990 A1$=RIGHT$(A1$,LEN(A1$)-4)         :'strip prefix (NDCV,VSRC,etc) from data
2000 A1$=LEFT$(A1$,LEN(A1$)-2)          :'remove terminator (<cr><lf>) from data
2010 RETURN
2020 PRINT "Device has an Overflow reading. Control C."
2030 STOP
2040 '============================================================
2050 '
2060 '       DIODE CURVES SUBROUTINE
2070 '
2080 GOSUB 1710                                 :'initialize the disk
2090    PRINT "CURRENT                                      VOLTAGE"
2100 CALL CNTL%(DEVLA$)                         :'device to listen
2110 A1$="C1XZ1XC0XF2R7T2M40X"                  :'zero device, ohms function,range
2120 FOR N=0 TO 5                               :'2 Gohms, one-shot trig on GET, and
2130    CALL TALK%(A1$)                         :'set SRQ for reading done & error
2140    CALL CNTL%(UNLI$)
2150    GOSUB 8690                              :'check if the reading is ready
2160    CALL CNTL%(DEVTA$)
2170    CALL LSTN%(A1$)                         :'obtain data
2180    CALL CNTL%(UNTA$)
2190    GOSUB 1960                              :'strip prefix and suffix
2200    R=VAL(A1$)
2210    I1=(10^N)*1E-09
2220    V1=I1*R
2230    V2=(LOG(V1))/2.30259
2240    I2=(LOG(I1))/2.30259
2250    PRINT #1,I1;:PRINT #1,I2;:PRINT #1,V1;:PRINT #1,V2   :'data to disk
2260    PRINT I1;"                              ";V1
2270    R8=6-N
2280    CALL CNTL%(DEVLA$)
2290    A1$="R"+STR$(R8)+"X"
2300 NEXT N
2310 A1$="Z0XC1X"
2320 CALL TALK%(A1$)
2330 CALL CNTL%(UNLI$)
2340 CLOSE #1
2350 INPUT "Press RETURN to continue.",A1$
2360 RETURN
2370 '
2380 '=============================================================================
2390 '          VOLTAGE VS CURRENT SUBROUTINE
2400 GOSUB 1710                                 :'Initiative the disk
2410 CALL CNTL%(DEVLA$)                         :'Device to listen
2420 A1$="C1XZ1XC0XF1R0T2M40X"                  :'Zero device Amps function
2430 CALL TALK%(A1$)                            :'Autorange, Trigger on Get, and set
2440 CALL CNTL%(UNLI$)                          :'SRQ for reading when done & error
2450 GOSUB 8010
```

```
2460 CLS
2470 VMIN$= " "                                :'VMAX$= " "
2480 ERCODE%=0
2490 PRINT "Voltage must be between +102 and -102 volts."
2500 INPUT "Starting Voltage ",V0
2510 INPUT "Ending Voltage ",V1
2520 INPUT "Increment size (50E-3 Volts minimum)", SZ
2525 VTEMP=V0 :VSAMP=V1 :FL=0
2530 IF SZ>ABS(V1-V0) THEN 2520
2540 IF V0>V1 THEN SZ = -SZ :VTEMP=V1 :VSAMP=V0 :FL=1
2550 N=1
2560 CLS
2570 PRINT "Voltage              Current"
2580 WHILE VTEMP <= VSAMP
2590      CALL CNTL%(DEVLA$)
2600      A1$="V"+STR$(V0)+"X"+"01XB0X"    :'Concatenate the voltage and
2610                                       :'set-up to take EM reading
2620      CALL TALK%(A1$)                  :'Output voltage to 617
2630      CALL CNTL%(GGET$)                :'Trigger device
2640      CALL CNTL%(UNLI$)
2650      GOSUB 8690                       :'Check if reading is ready
2660      CALL CNTL%(DEVTA$)
2670      CALL LSTN%(A1$)                  :'Obtain data
2680      CALL CNTL%(UNTA$)
2690      GOSUB 1960                       :'Strip prefix & suffix
2700      CURR$=A1$
2710      A1$="00XB4X"
2720      CALL CNTL%(DEVLA$)               :'Have 617 shut off Voltage source
2730      CALL TALK%(A1$)                  :'and set-up to get voltage output
2740      CALL CNTL%(UNLI$)
2750      CALL CNTL%(DEVTA$)
2760      CALL LSTN%(A1$)                  :'Get voltage source output value
2770      CALL CNTL%(UNTA$)
2780      GOSUB 1960                       :'Strip prefix & suffix
2790      VOLT$=A1$
2800      PRINT VOLT$+"          "+CURR$   :'Print to screen
2810      V2=VAL(VOLT$)
2820      I2=VAL(CURR$)
2830 IF V2>0 THEN V3=LOG(V2) ELSE V3=0
2840 IF I2>0 THEN I3=LOG(I2) ELSE I3=0
2845      IF I2>0 THEN I4=SQR(I2) ELSE I4=0
2850      PRINT #1,I2;I3;I4;V2;V3              :'Print to disk
2860      V0=V0+SZ
2862      IF FL = 1 THEN VSAMP=V0 :GOTO 2870
2864      VTEMP = V0
2870      N=N+1
2880      IF N<=20 THEN 2930
2890      N=1
2900      INPUT "Press RETURN to continue", A1$
2910      CLS
2920      PRINT "VOLTAGE              CURRENT"
2930 WEND
```

```
2940 CLOSE #1
2950 A1$="C1X"
2960 CALL CNTL%(DEVLA$)
2970 CALL TALK%(A1$)
2980 CALL CNTL%(UNLI$)
2990 INPUT "Press RETURN to continue",A1$
3000 RETURN
8000 '
8010 ' ============================================================
8020 '           Report 488 Function Errors
8030 '
8040 '
8050 ' Interpret Error codes and print error messages
8060 '
8070 IF ERCODE%<0 THEN 8410
8080 IF ERCODE%=0 THEN RETURN
8090 IF ERCODE%>255 THEN 8410
8100 PRINT "Error code = ";ERCODE%
8110 FOR I=7 TO 0 STEP -1
8120 I0=2^I
8130 R9=ERCODE%-I0 : IF R9 < 0 THEN 8370
8140 ERCODE%=R9
8150 ON I+1 GOTO 8170,8200,8220,8250,8280,8310,8330,8350
8160 '
8170 PRINT "SETUP ERROR - either IOSET% or PROTCL% wasn't called before"
8180 PRINT "               using one of the MSOFT communication functions".
8190 GOTO 8370
8200 PRINT "NO LISTENERS - I cannot talk to myself!"
8210 GOTO 8370
8220 PRINT "SERIAL POLL ADDRESS ERROR - no more than one secondary address"
8230 PRINT "                            may follow a primary address"
8240 GOTO 8370
8250 PRINT "SERVICE REQUEST - a 488 device is requesting service"
8260 GOSUB 8690
8270 ERCODE%=0 :RETURN
8280 PRINT "TIMEOUT ERROR - the specified amount of time has elapsed without"
8290 PRINT "                completing a 488 handshake cycle"
8300 GOTO 8370
8310 PRINT "ATN TRUE - an external controller is trying to issue a command"
8320 GOTO 8370
8330 PRINT "IFC TRUE - reset 488 interface"
8340 GOTO 8370
8350 PRINT "S-100 RESET - reset interface (CONTROL C)"
8360 GOTO 8370
8370 NEXT I
8380 PRINT "Error condition must be corrected before continuing. Enter ^C."
8390 STOP
8400 RETURN
8410 PRINT "SYSTEM ERROR - an illegal error code has been encountered"
8420 RETURN
8430 '
8440 '  ============================================================
```

```
8450 '                        String Input Routine
8460 '
8470 '  Get the string.  Gather control codes if preceded by <ESCAPE>.
8480 '
8490 A1$=""
8500 GOSUB 9220 'MACHINE LANGUAGE INPUT ROUTINE
8510 IF ASC(A8$)<>13 THEN 8540  : '  <RETURN> terminates input
8520 PRINT
8530 RETURN
8540 '  Use backspace key for character at a time deletion
8550 IF ASC(A8$)=8 THEN IF LEN(A1$)>0 THEN 8570 ELSE 8500
8560 GOTO 8630
8570 A9$=RIGHT$(A1$,1)                    : '  keep deleted char
8580 A1$=LEFT$(A1$,LEN(A1$)-1)            : '  remove deleted char from string
8590 PRINT CHR$(8);" ";CHR$(8);           : ' delete char from CRT
8600 '  If deleted char is a control char must also delete leading caret
8610 IF ASC(A9$)<32 THEN PRINT CHR$(8);" ";CHR$(8);
8620 GOTO 8500
8630 IF ASC(A8$)=27 THEN GOSUB 9220 : '  <ESCAPE> means get next char
8640 '  Show the control character.  If not a space preceed character with
8650 '  a caret.  Change the control character into a printing character.
8660 IF A8$>=" " THEN PRINT A8$; ELSE PRINT "^"+CHR$(64+ASC(A8$));
8670 A1$=A1$+A8$    : '  Append the character to the string
8680 GOTO 8500
8690 '
8700 '  ============================================================
8710 '           SERIAL POLL SUBROUTINE
8720 S=0
8730 A1$="["
8740 S=S+1
8750 CALL SPOLL%(A1$,B1$)
8760 IF S>20 THEN RETURN
8770 R9=POLL% - 128 :IF R9>0 THEN POLL%=R9
8780 R9=POLL%-64 :IF R9<0 THEN 8730      :'Was an SRQ generated
8790 POLL%=R9
8800 FOR I=5 TO 0 STEP -1
8810   S=2^I
8820   R9=POLL% - S :IF R9 < 0 THEN 9050
8830   POLL%=R9
8840   ON I+1 GOTO 9040,9040,9050,9030,9050,8850
8850 CALL CNTL%(DEVLA$)                   :'Error!
8860 A1$="U1X"
8870 CALL TALK%(A1$)
8880 CALL CNTL%(UNLI$)
8890 CALL CNTL%(DEVTA$)
8900 CALL LSTN%(A1$)                      :'Obtain status word
8910 CALL CNTL%(UNTA$)
8920 A1$=RIGHT$(A1$,LEN(A1$)-3)           :'Strip 617 from status
8930 A1$=LEFT$(A1$,LEN(A1$)-5)            :'Strip trailing zeroes & terminator
8940 CHK$=LEFT$(A1$,2)
8950 IF VAL(CHK$)=0 THEN 8960 :PRINT "IDDC or IDDCO error."
```

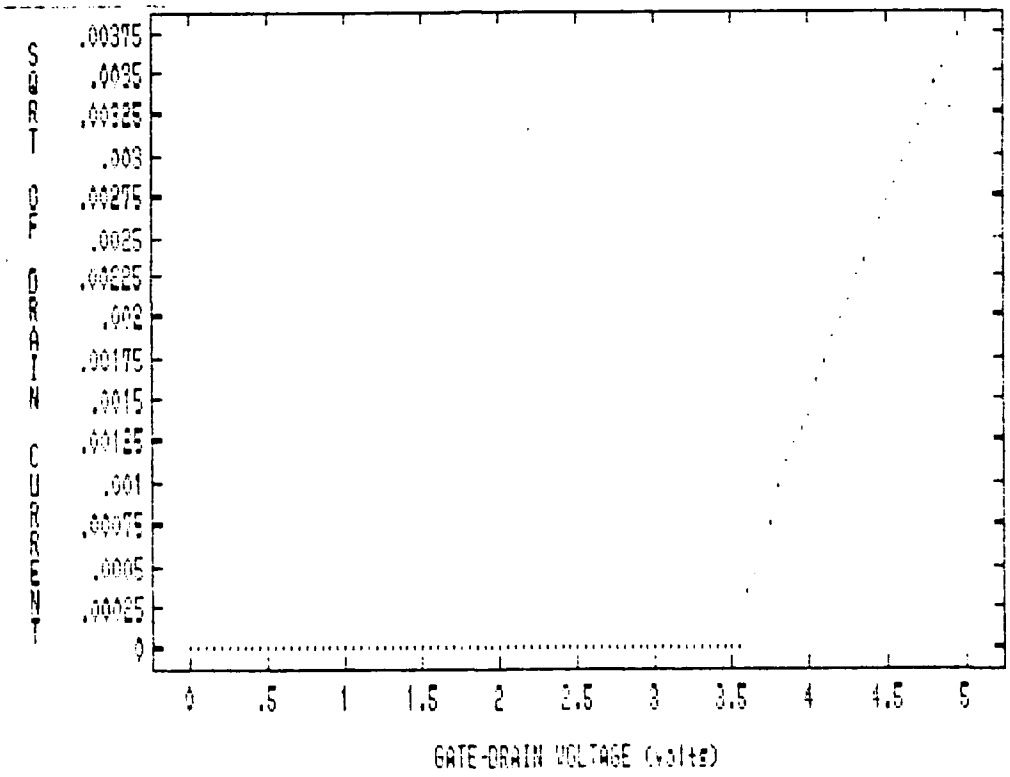
```
8960 CHK$=RIGHT$(A1$,1)
8970 IF VAL(CHK$)=0 THEN 8980 :PRINT "Out of range voltage source value."
8980 CHK$=RIGHT$(A1$,2)
8990 IF VAL(CHK$)>9 THEN PRINT "Trigger overrun."
9000 PRINT "Error code word is ";A1$
9010 INPUT "You should consider aborting the run if an error exists.",A1$
9020 GOTO 9050
9030 GOTO 9050
9040   PRINT "DATA STORE FULL or OVERRANGE INPUT"
9050 NEXT I
9060 RETURN
9070 '
9080 'LOAD MACHINE LANGUAGE SUBROUTINE
9090 '
9100 '
9110 DATA B4,07,CD,21,8B,EC,8B,5E
9120 DATA 04,43,8B,1F,88,07,CA,02,00
9130 '
9140 DIM GETKEY(4)
9150 FOR I=1 TO 17
9160 READ X$:X=VAL("&H"+X$)
9170 BYTE=VARPTR(GETKEY(0)):POKE BYTE+I-1,X
9180 NEXT I
9190 '
9200 RETURN
9210 '
9220 A8$=" "+"":PRINT CHR$(27);"y5";:KEYIN=VARPTR(GETKEY(0)):CALL KEYIN(A8$):PRI
NT CHR$(27);"x5";    'MACHINE LANGUAGE INKEY$:RETURNS ALL ESCAPE CHARACTERS
9230 RETURN
```

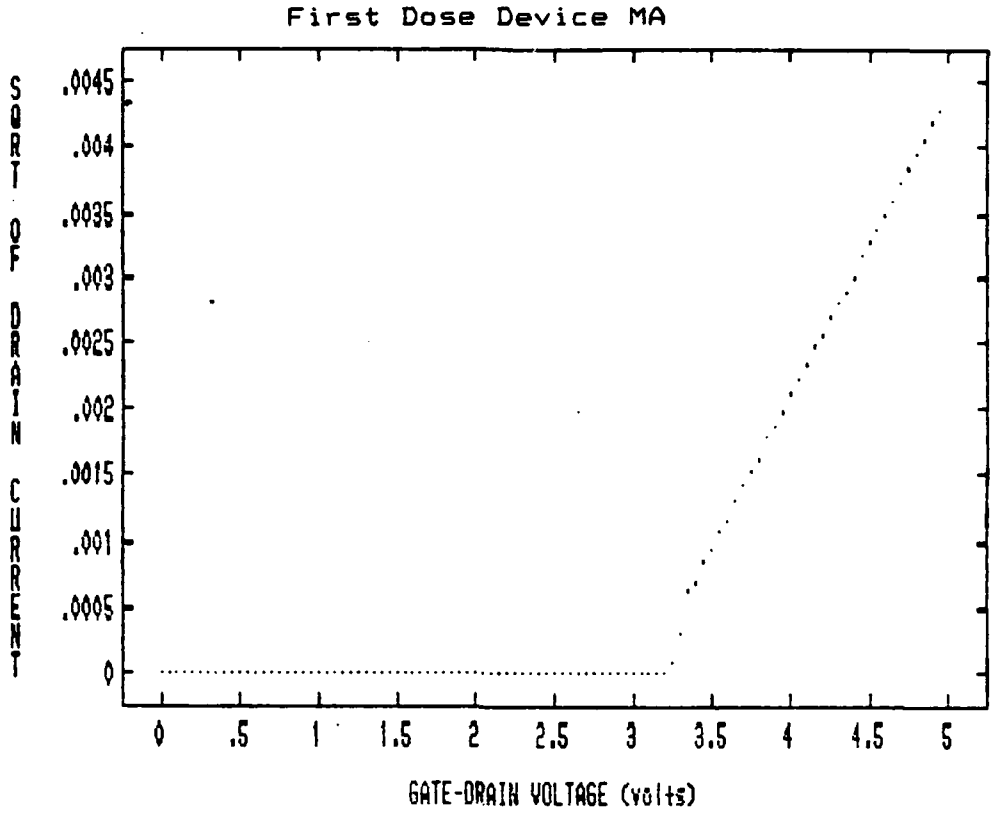
APPENDIX D

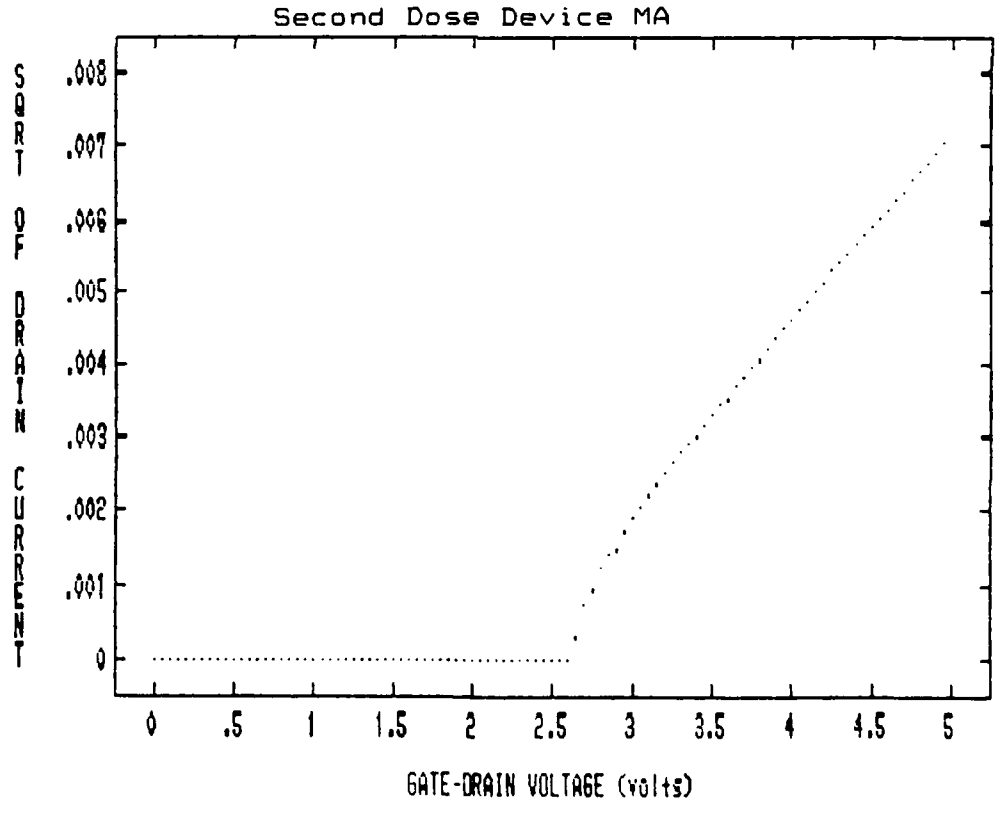
RAW DATA GRAPHS

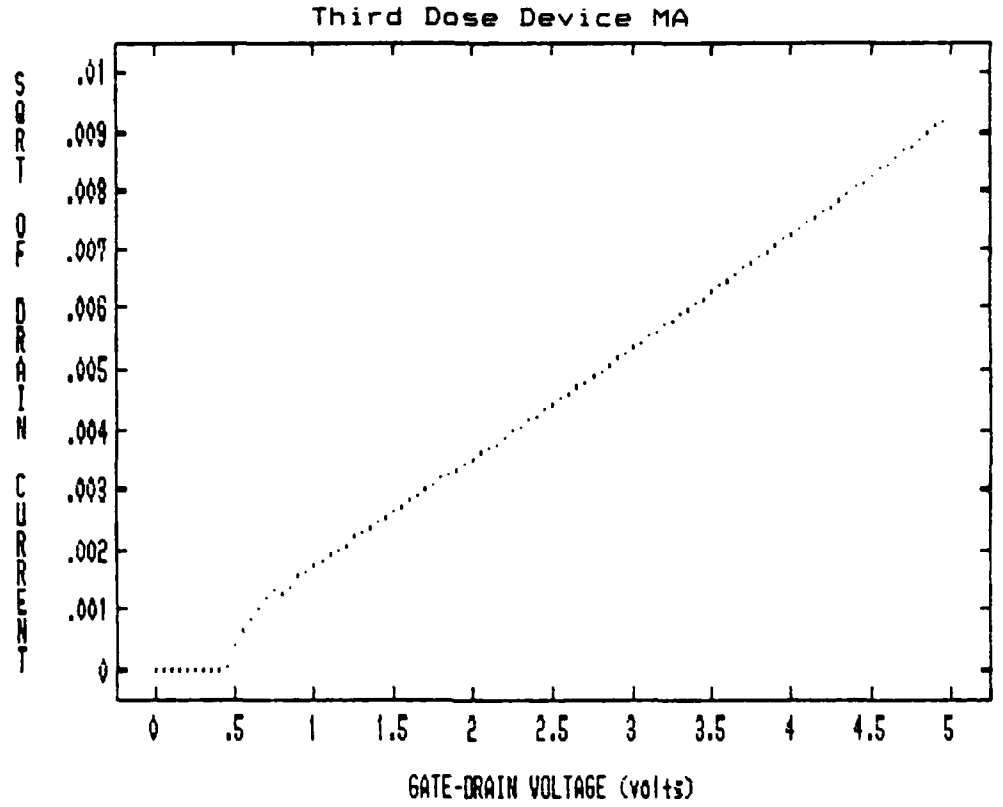
The following graphs were used to obtain the threshold voltage and transconductance data tabulated in Chapter IV. The doses referred to in the graph titles are those of Tables 4-1 and 4-2. The y-axis of each graph is in units of square root of amps.

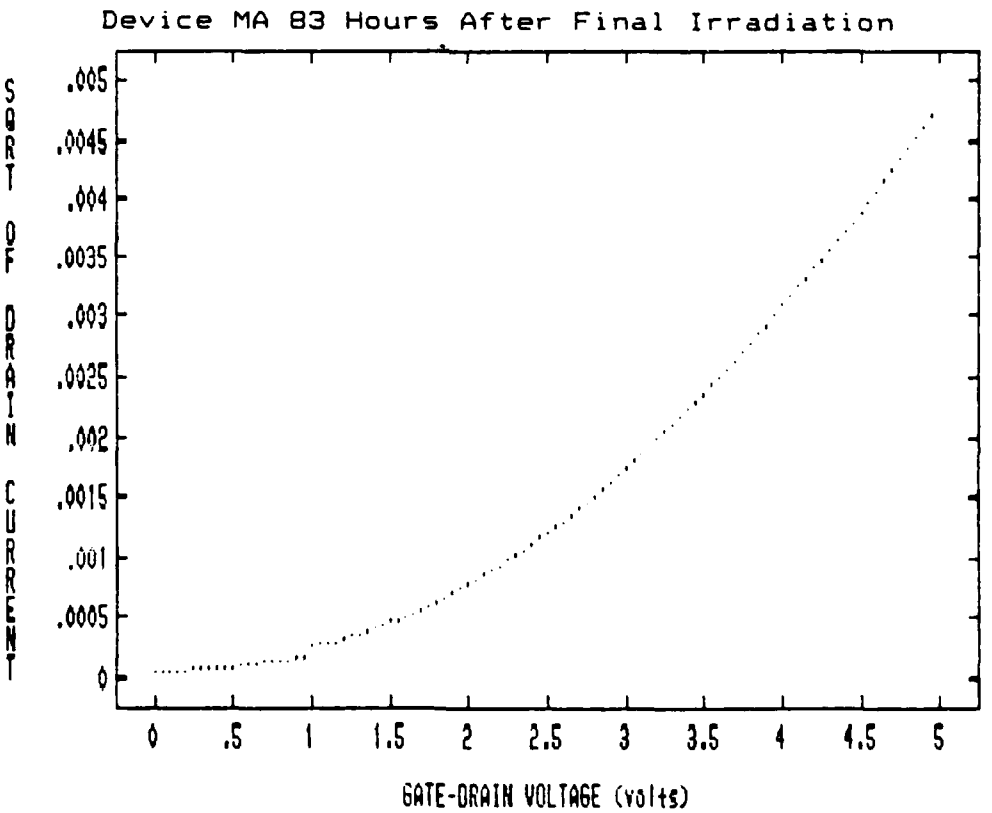
Pre-radiation Device MA



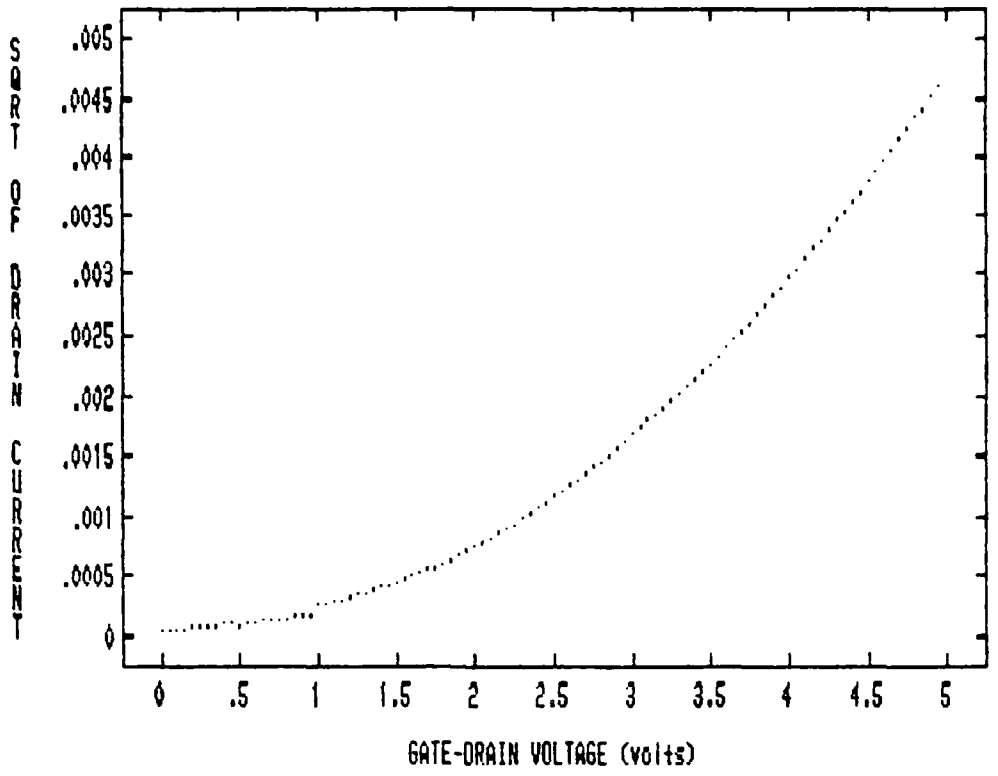




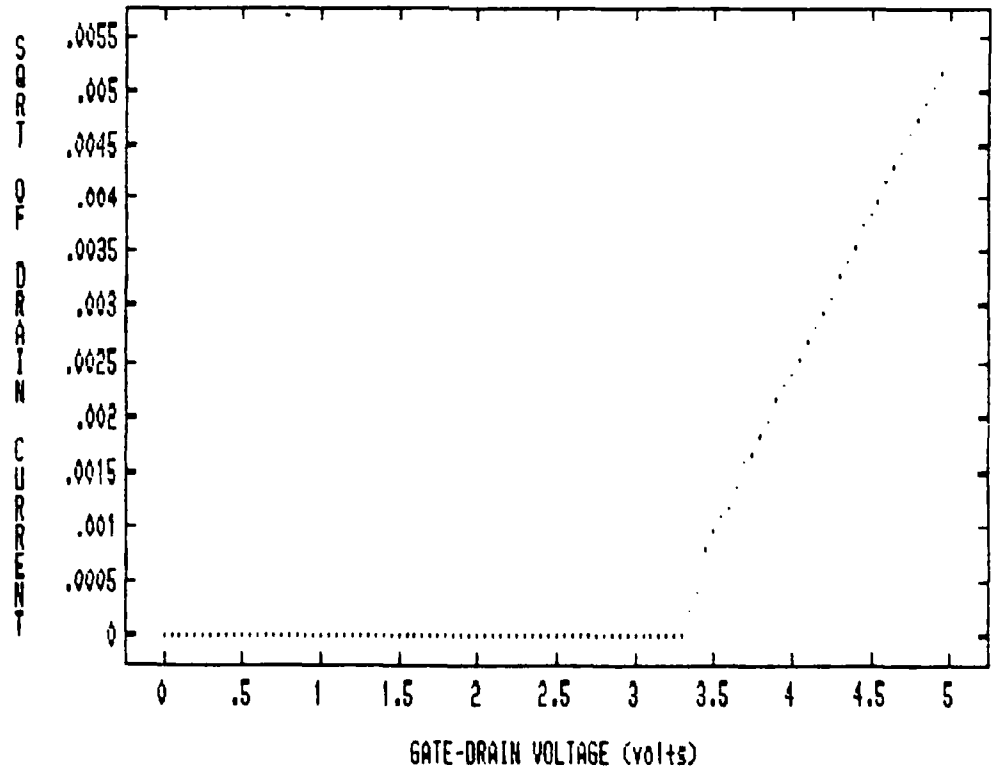


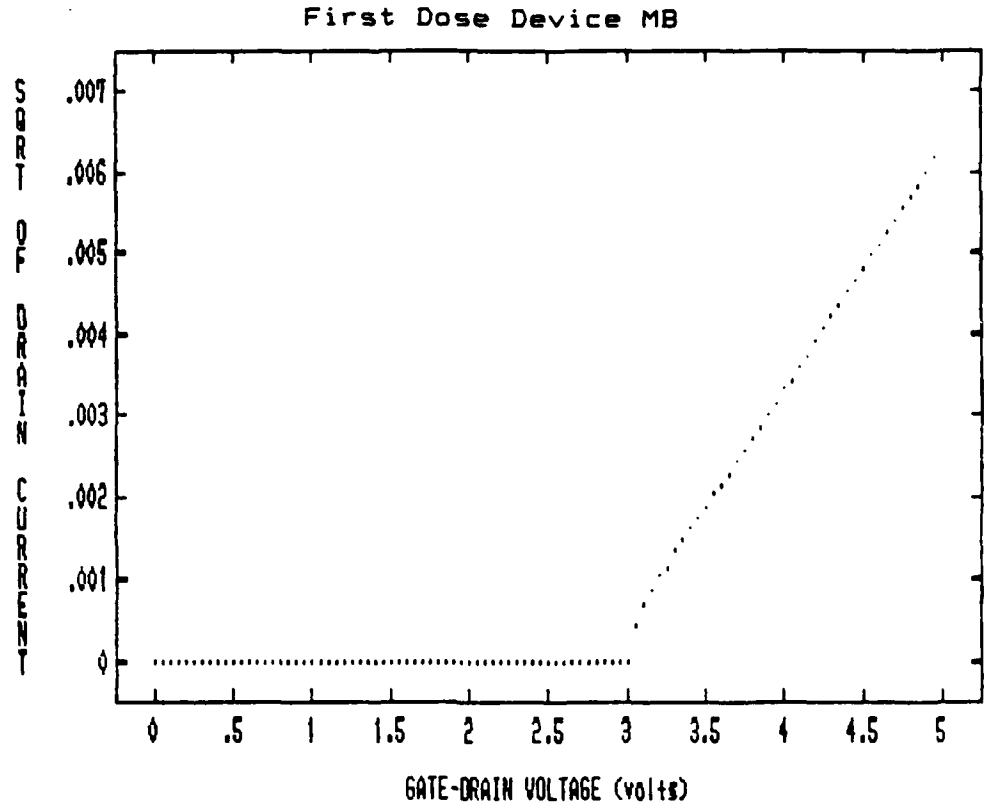


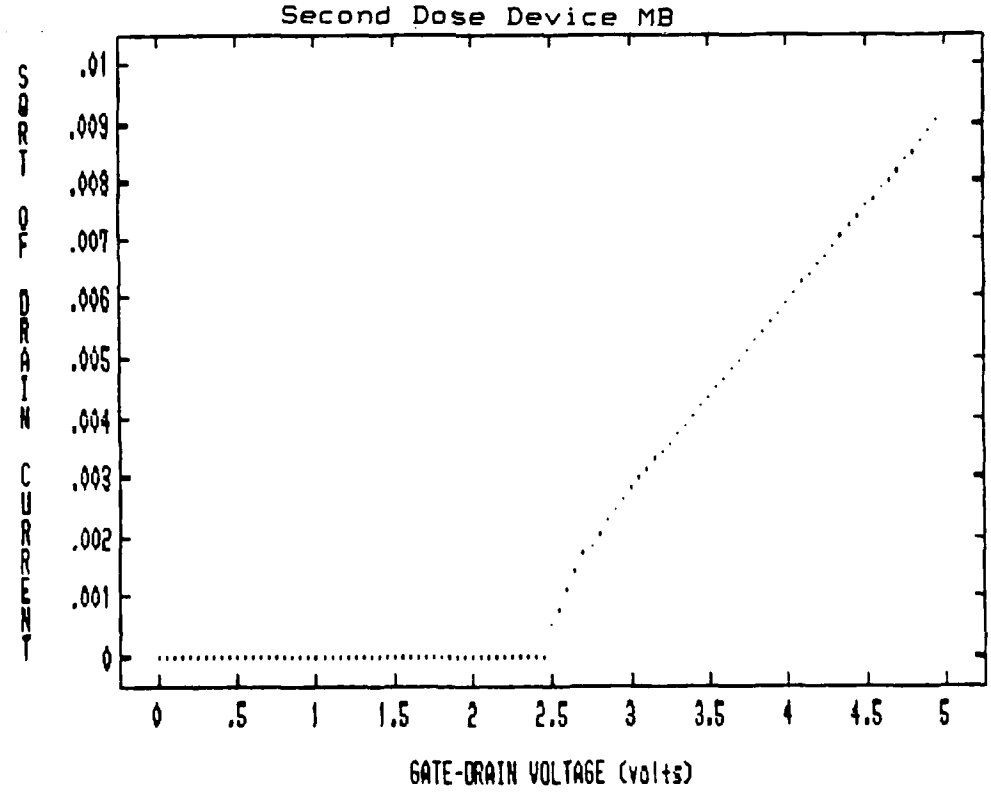
Device MA 107 Hours After Final Irradiation

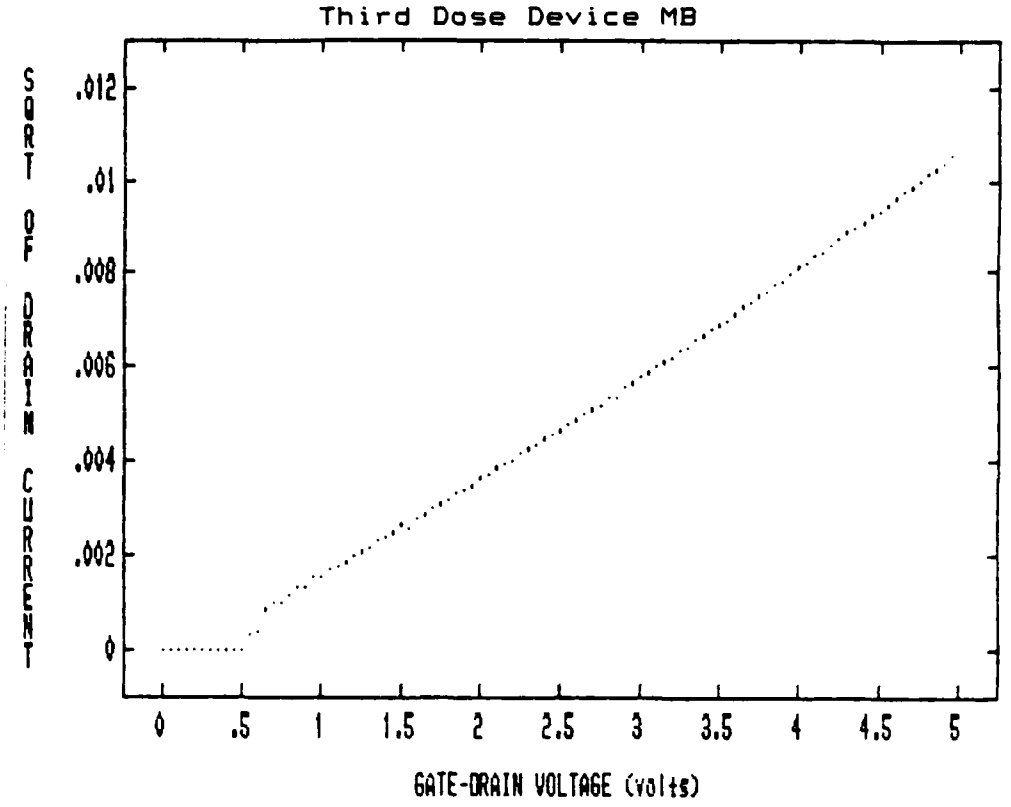


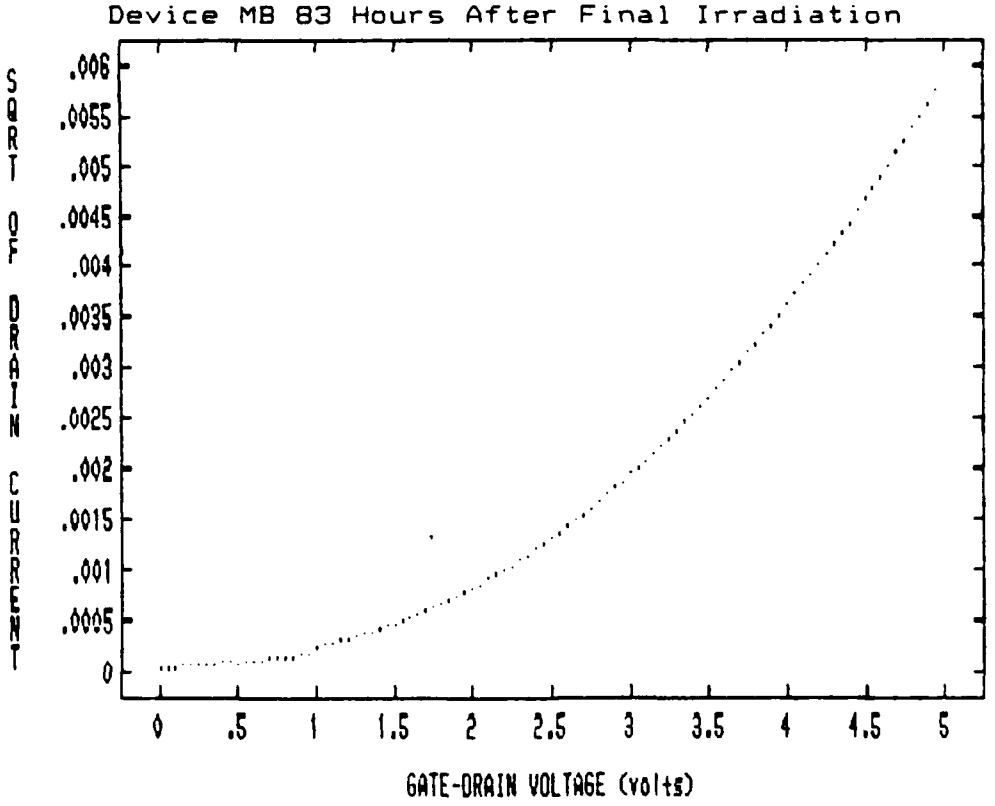
Pre-radiation Device MB



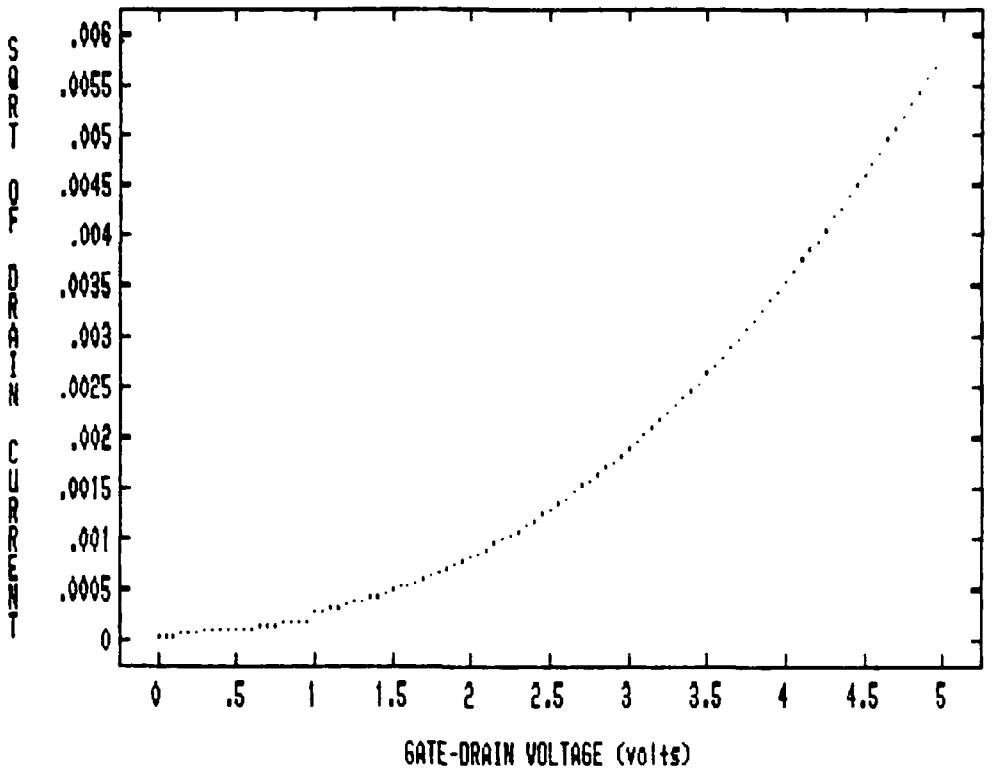




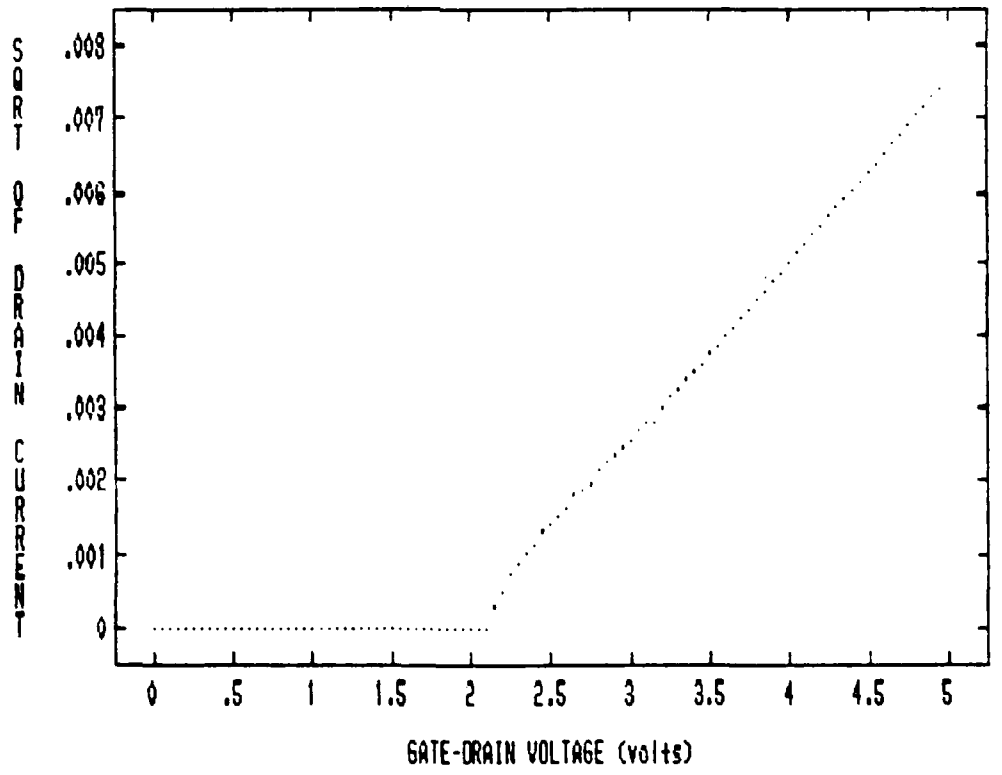


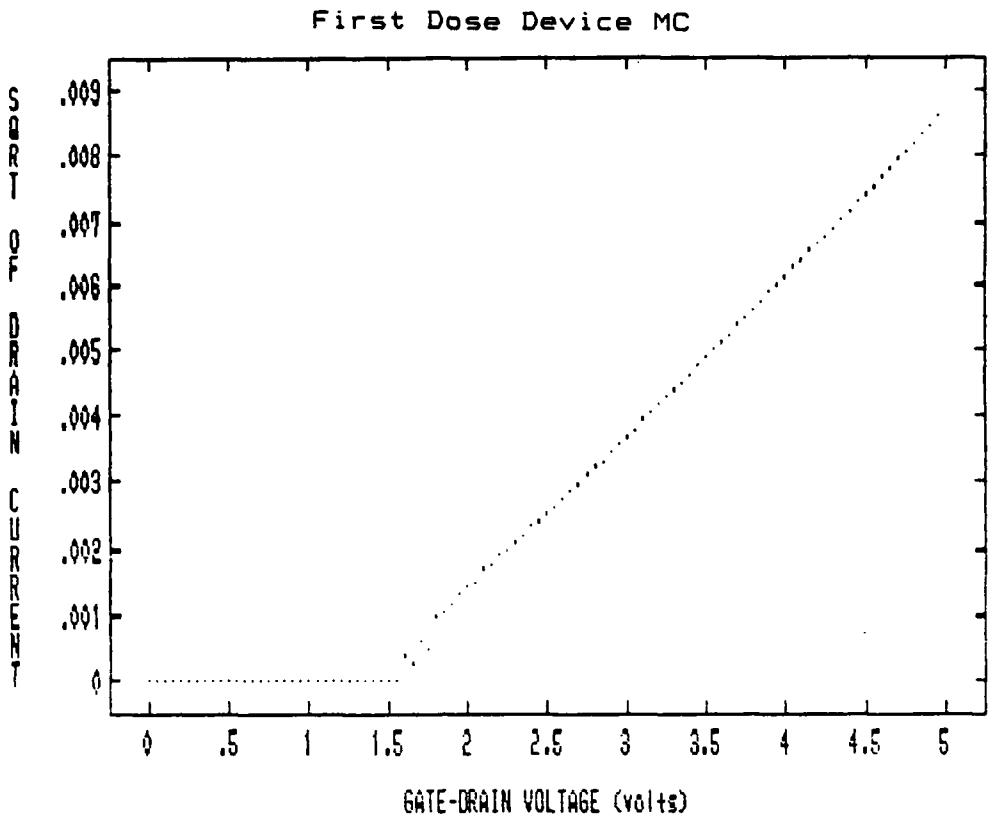


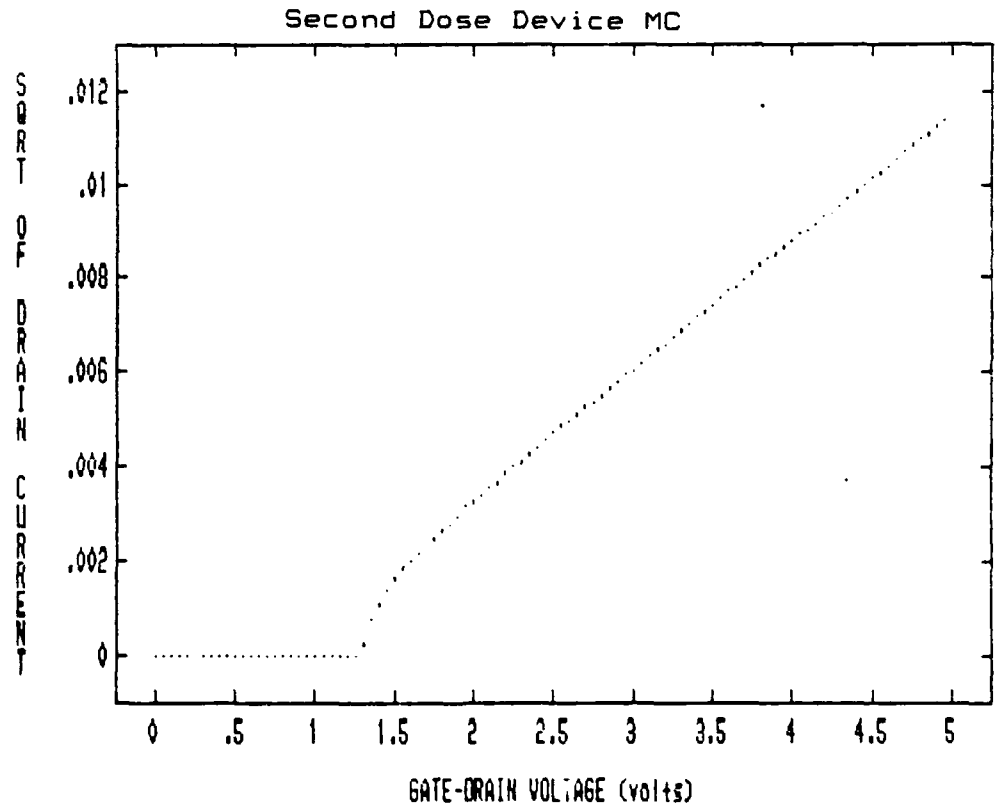
Device MB 107 Hours After Final Irradiation

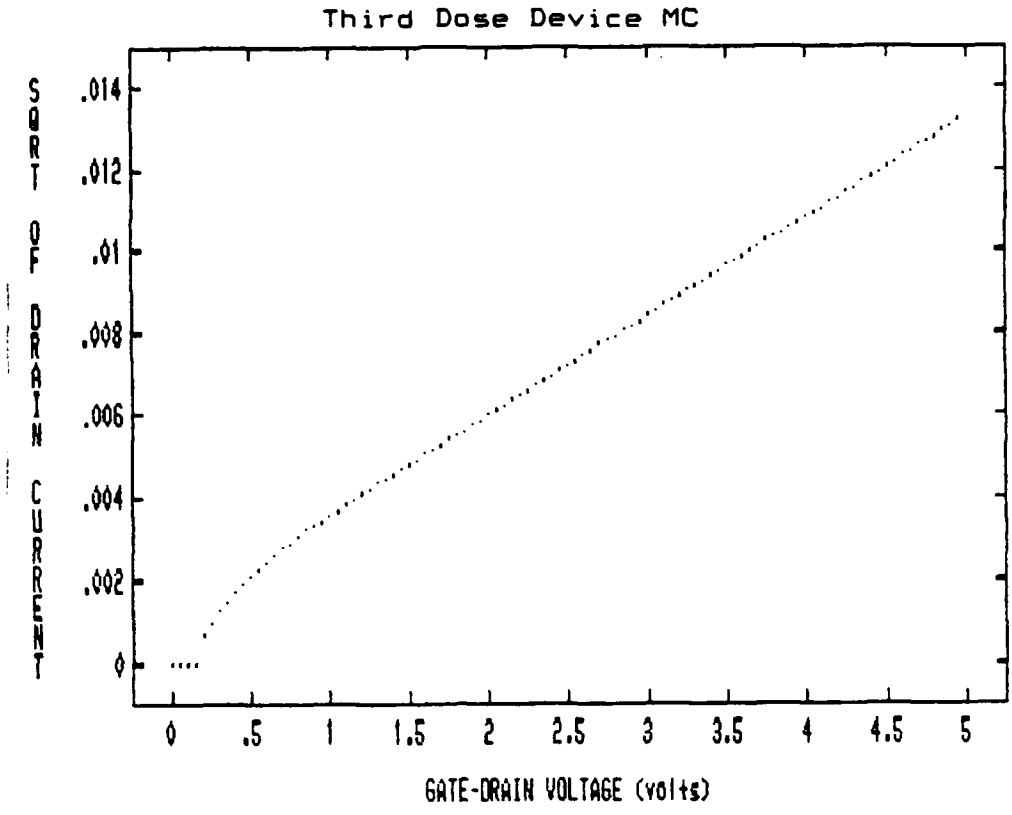


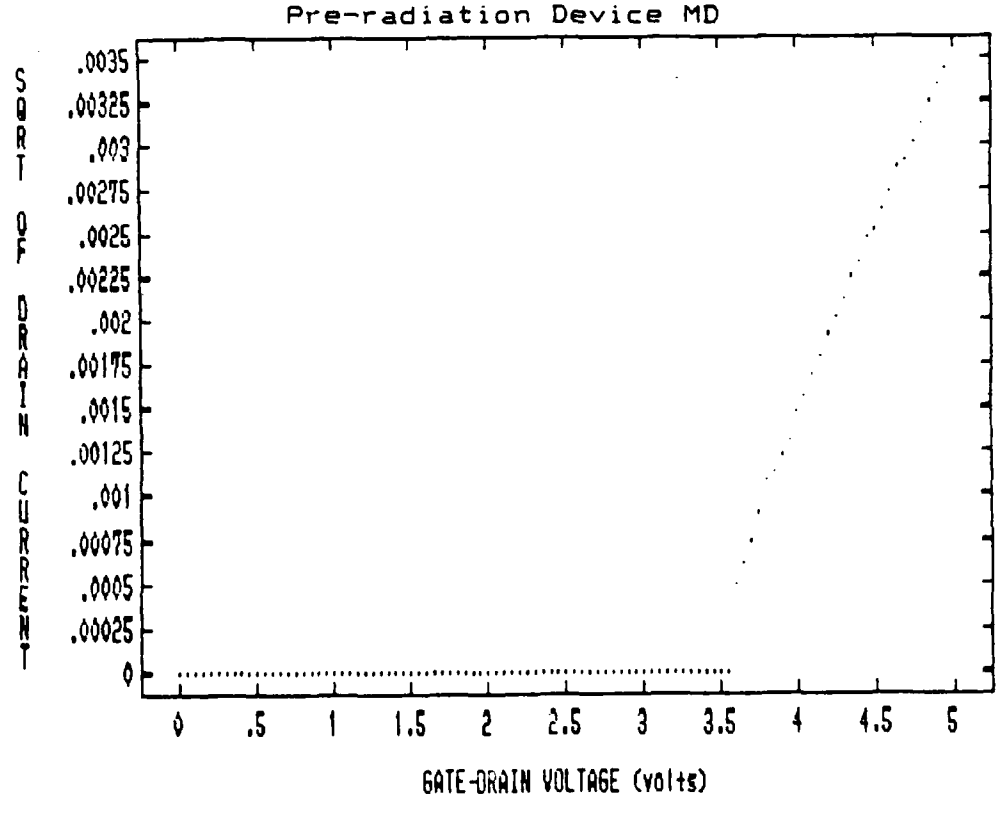
Pre-radiation Device MC

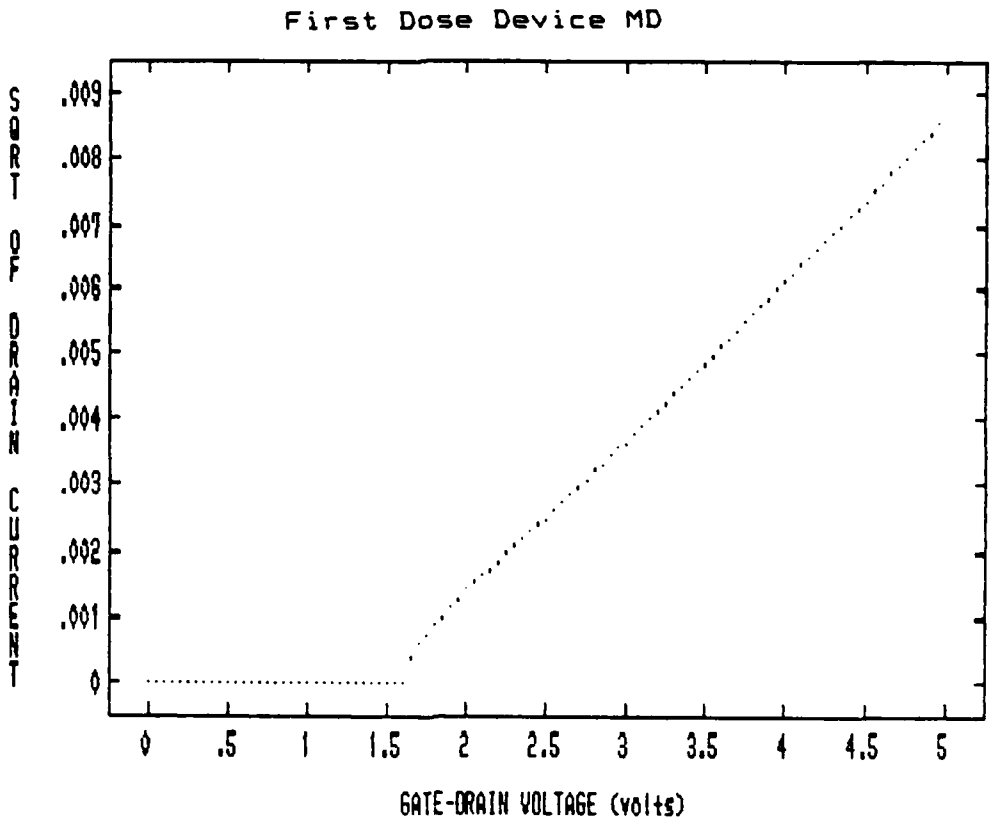


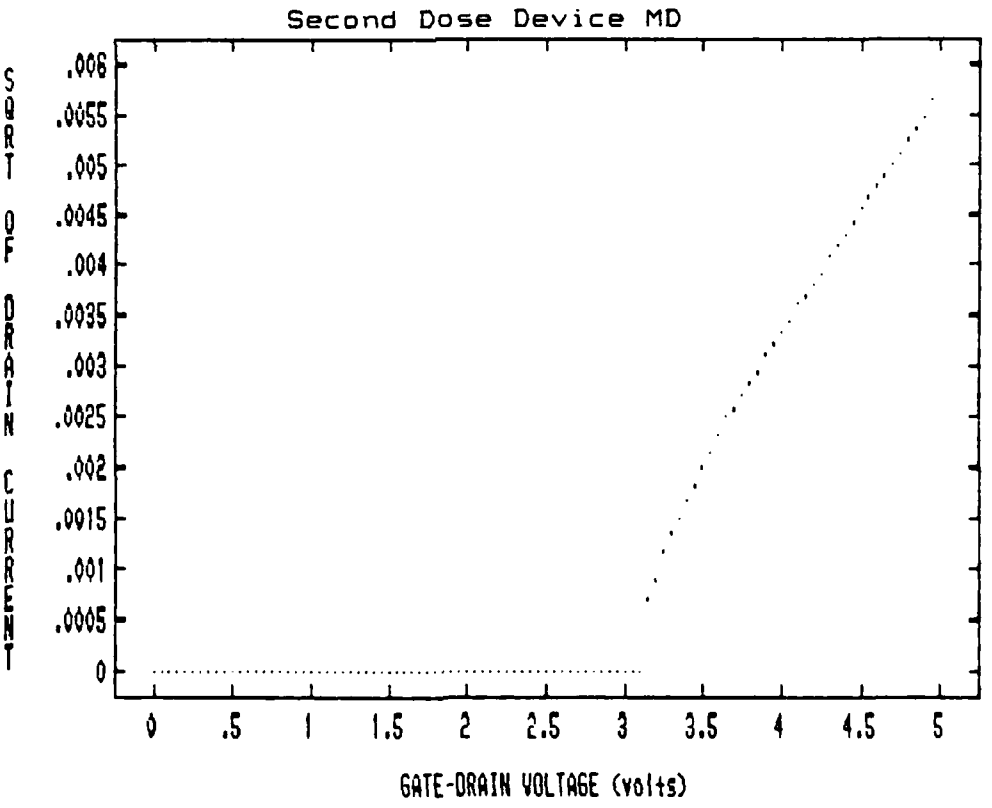


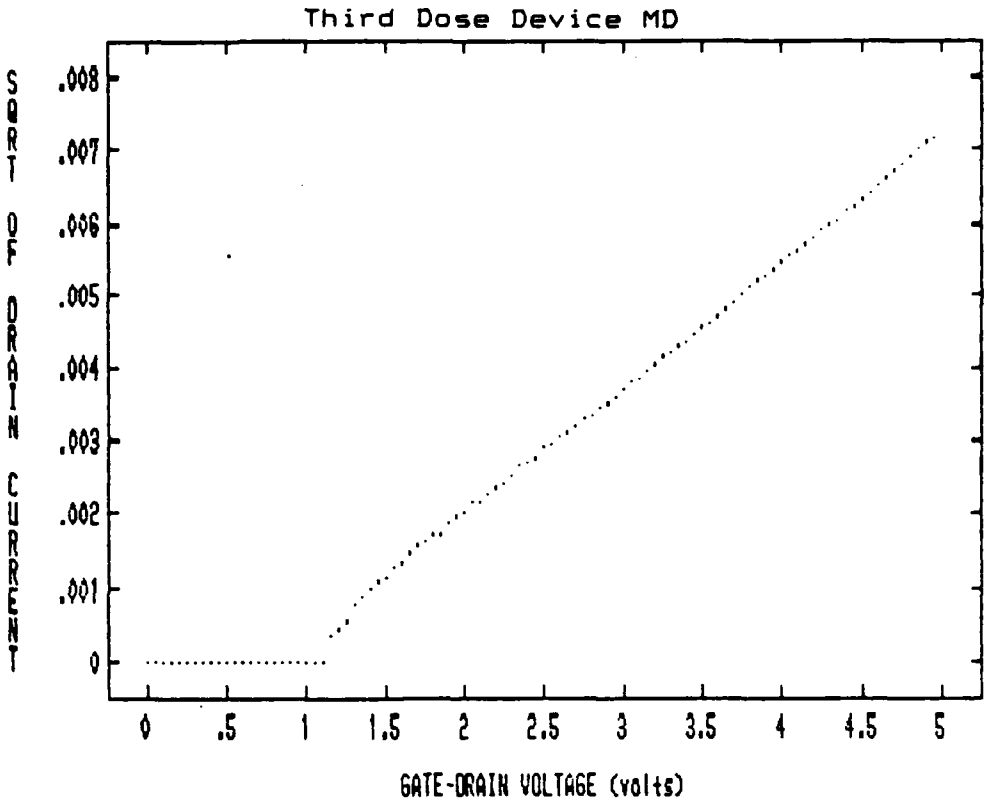


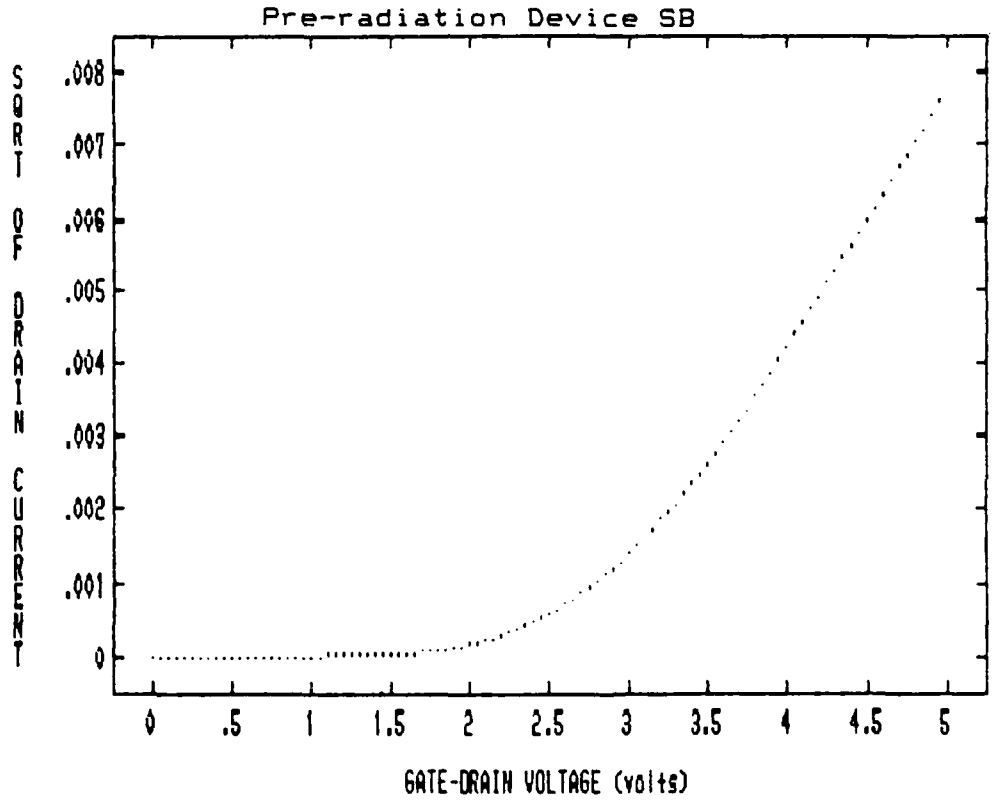




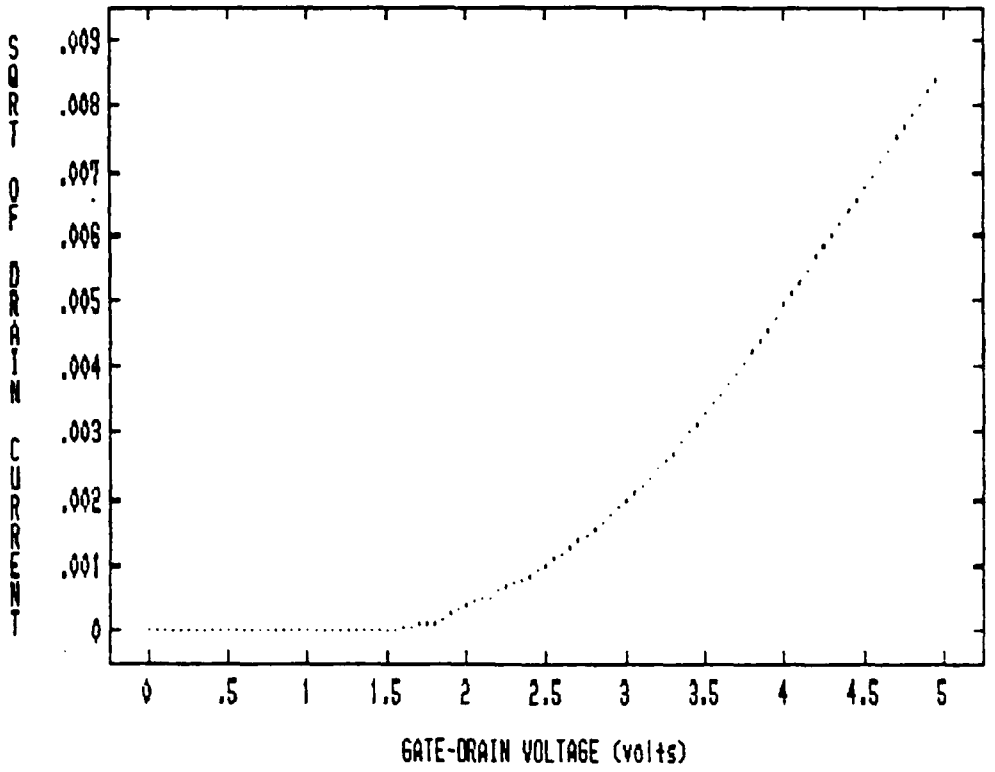








First Dose Device SB



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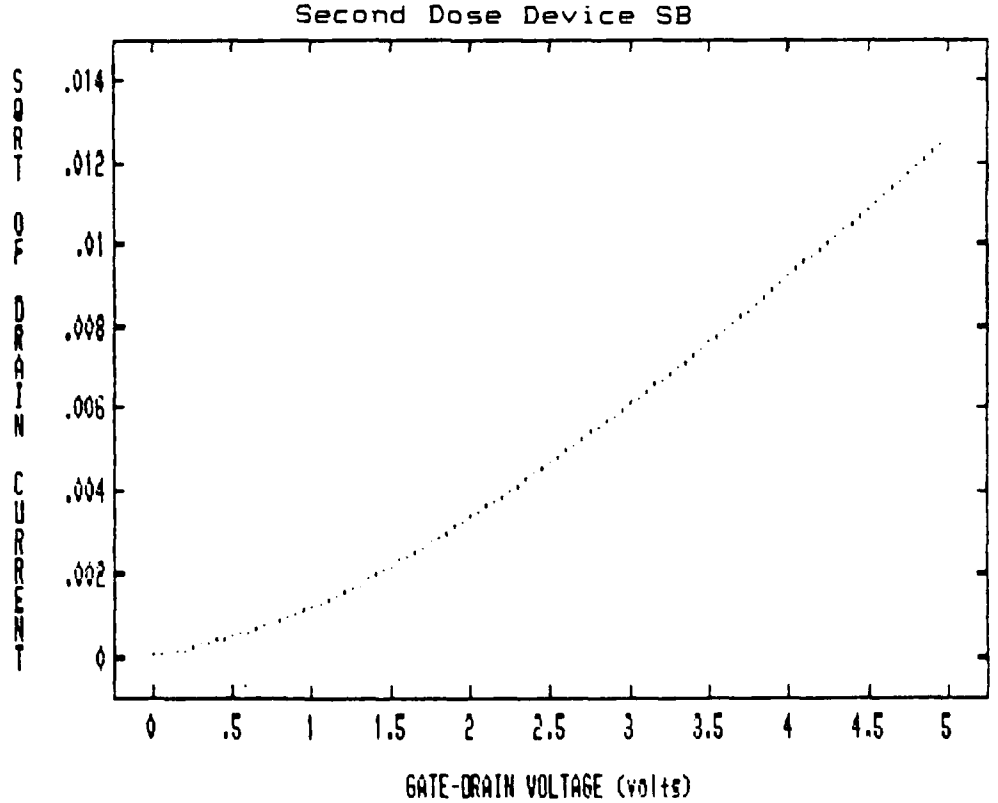

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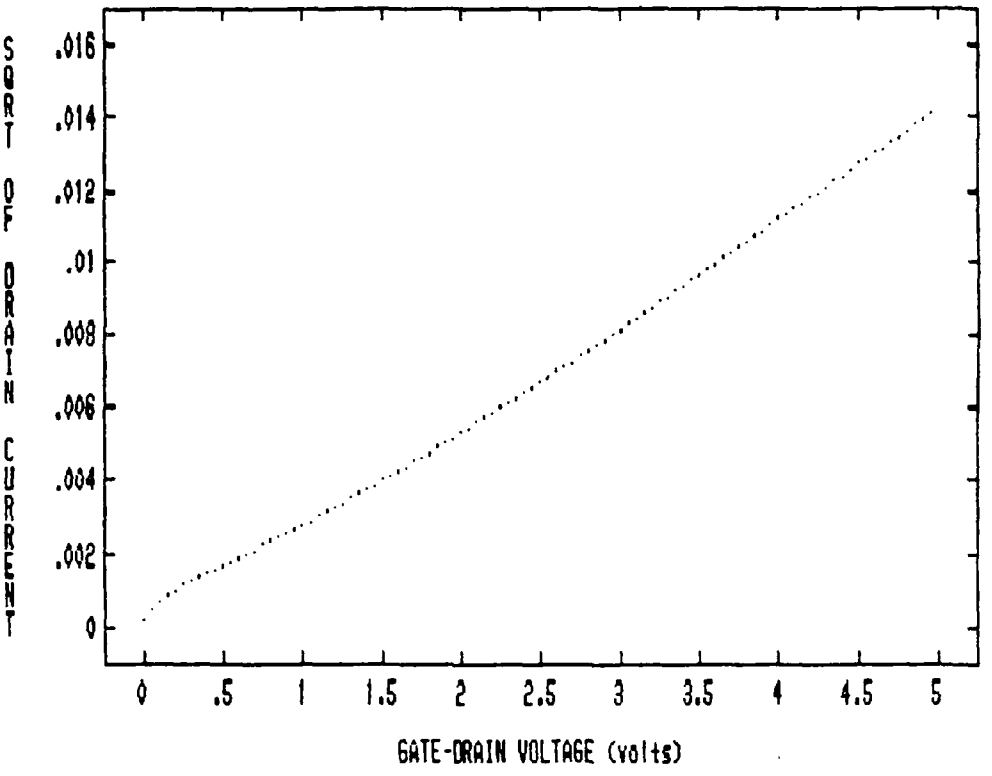

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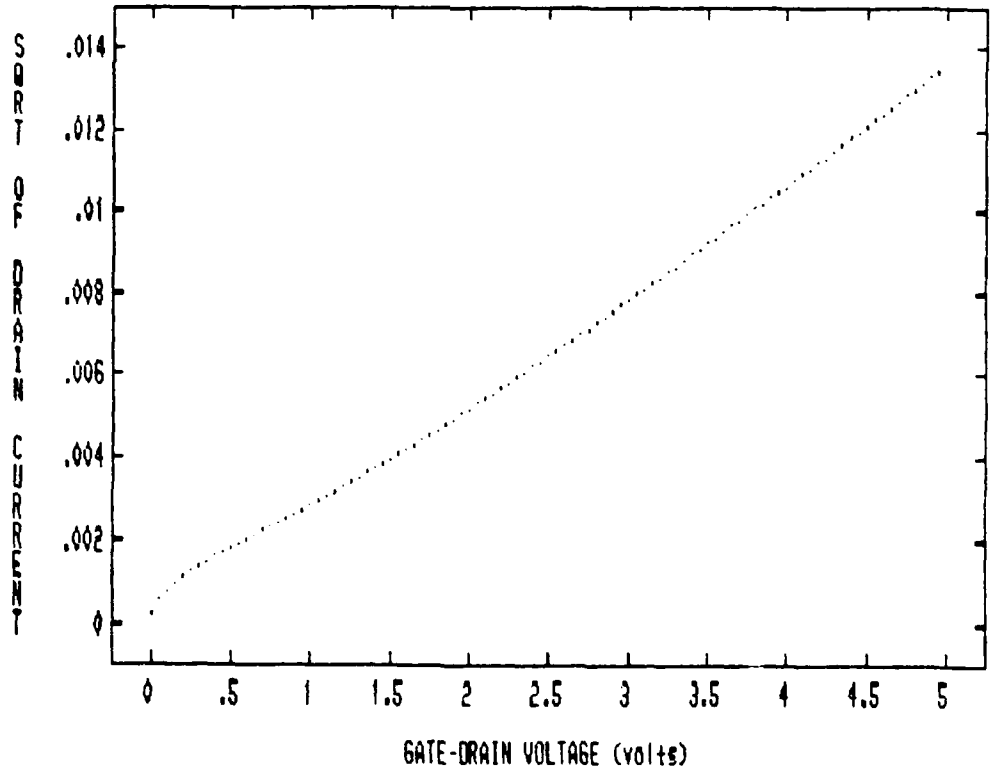

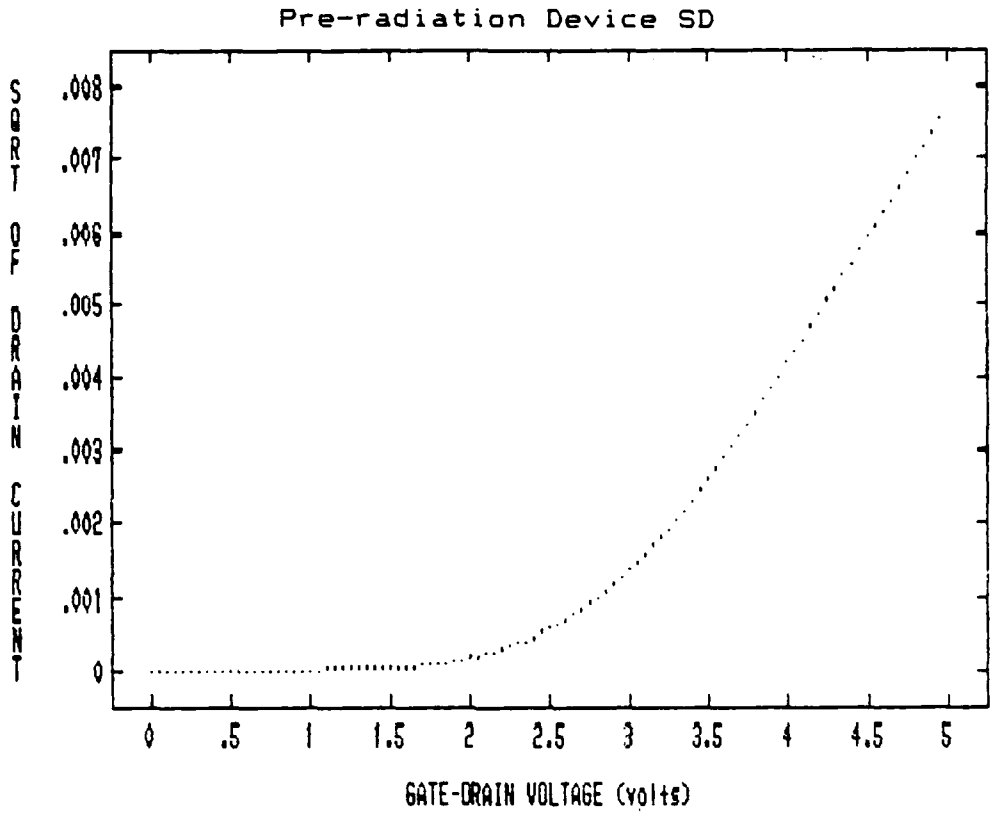

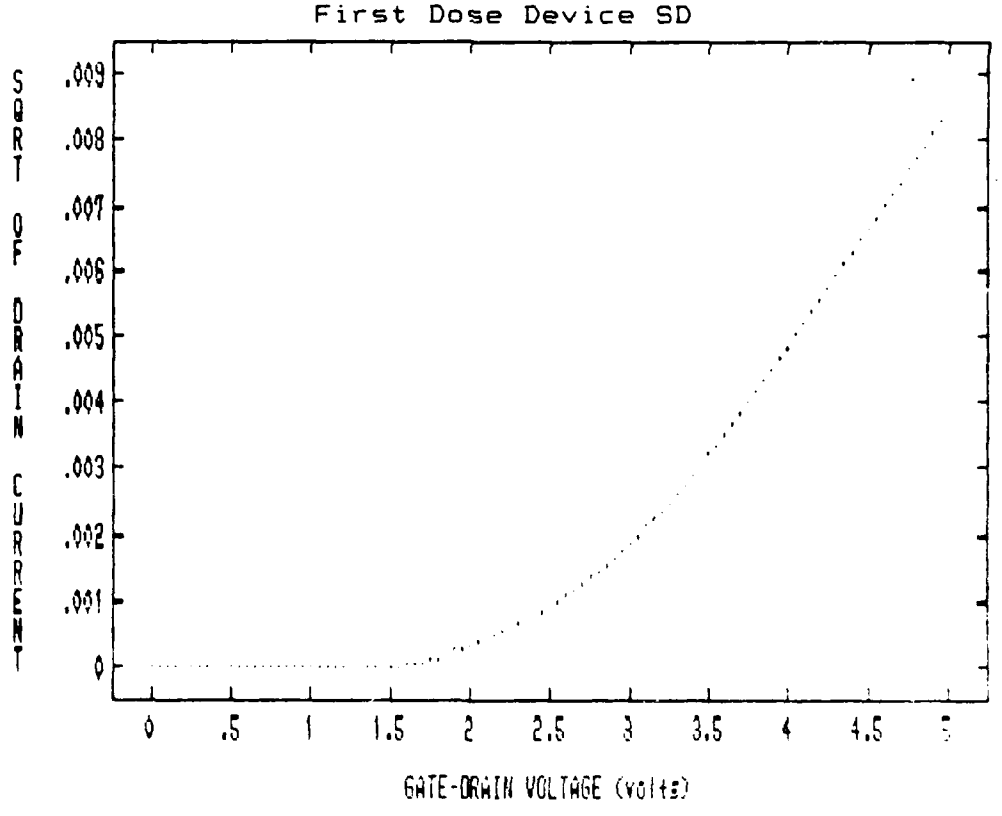

AD-A164 520 ELECTRON IRRADIATION OF N CHANNEL SILICON ON SAPPHIRE INSULATED GATE FIELD EFFECT TRANSISTORS (IGFET)(U) NAVAL POSTGRADUATE SCHOOL MONTEREY CA R A PORNARAS

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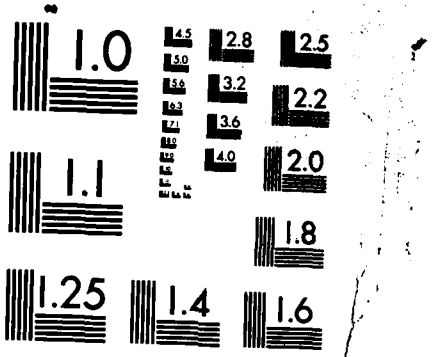
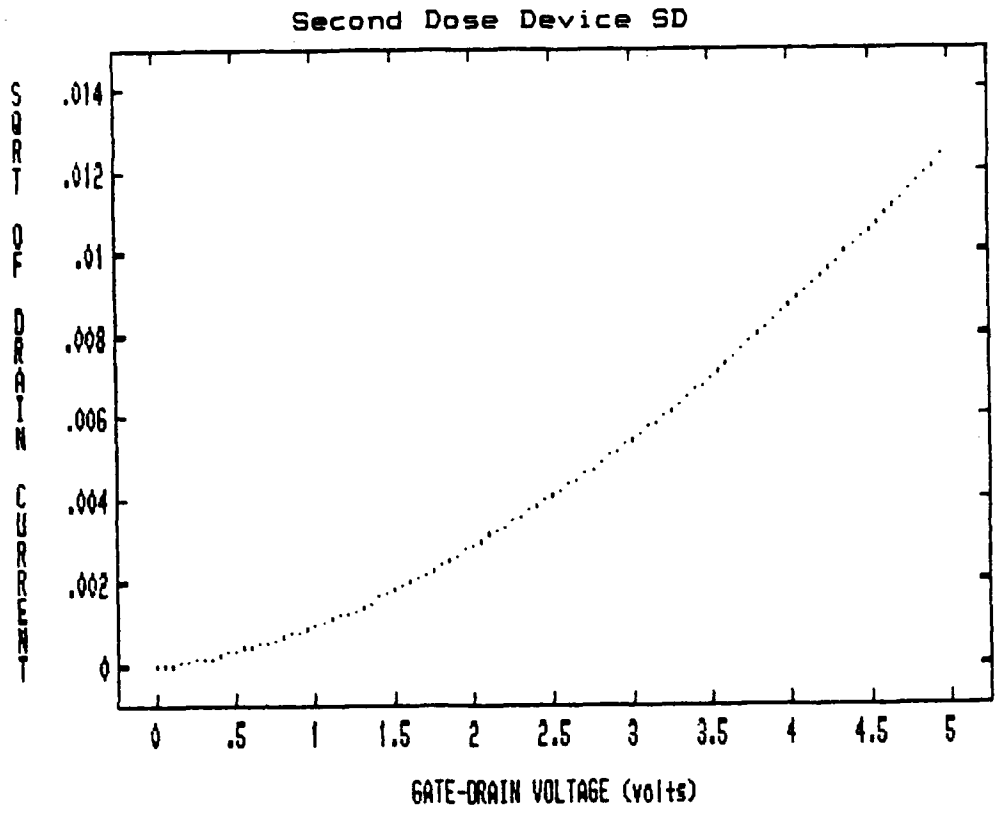
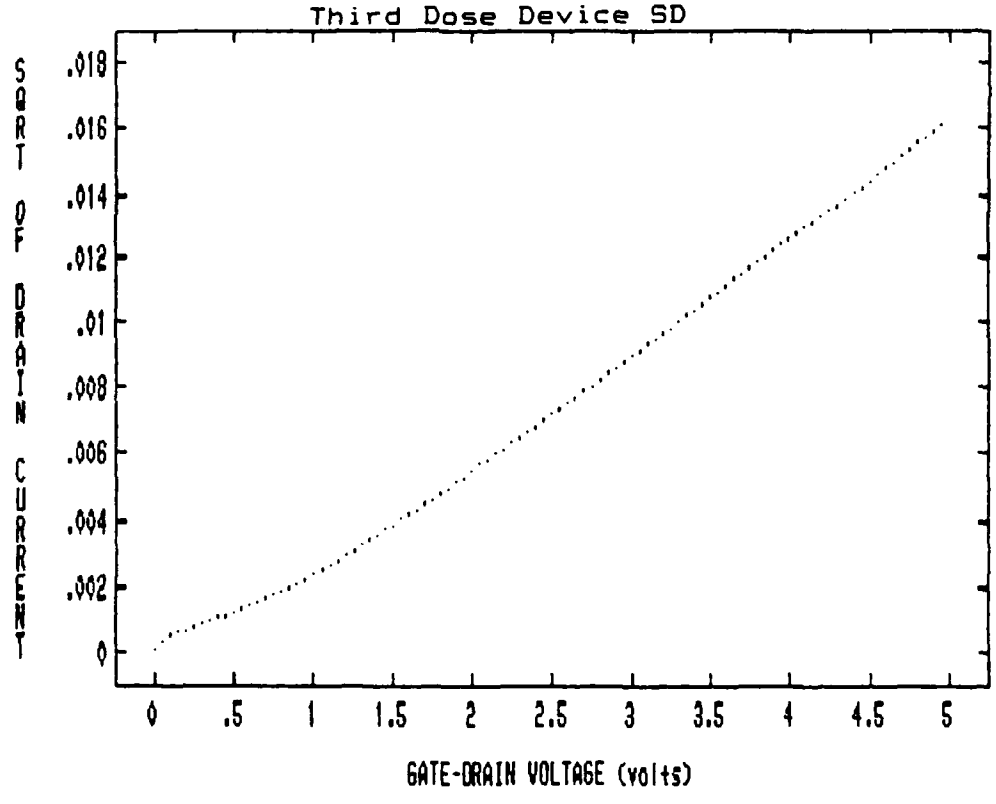
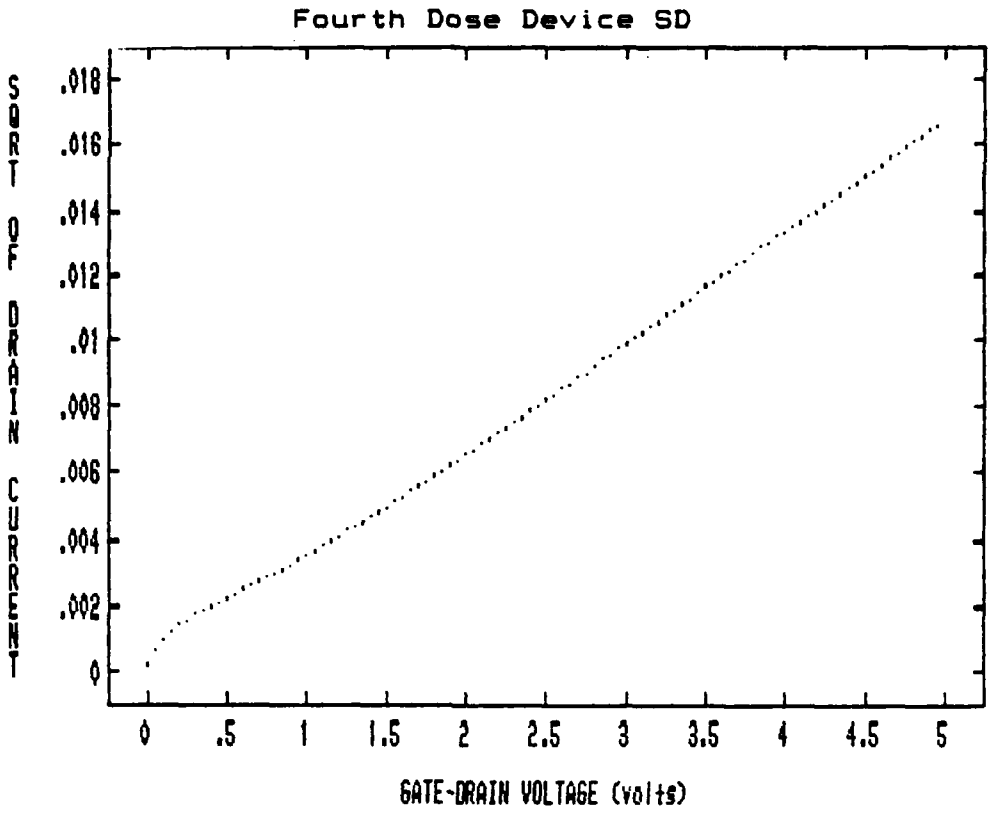
UNCLASSIFIED DEC 85 F/G 9/1 NL

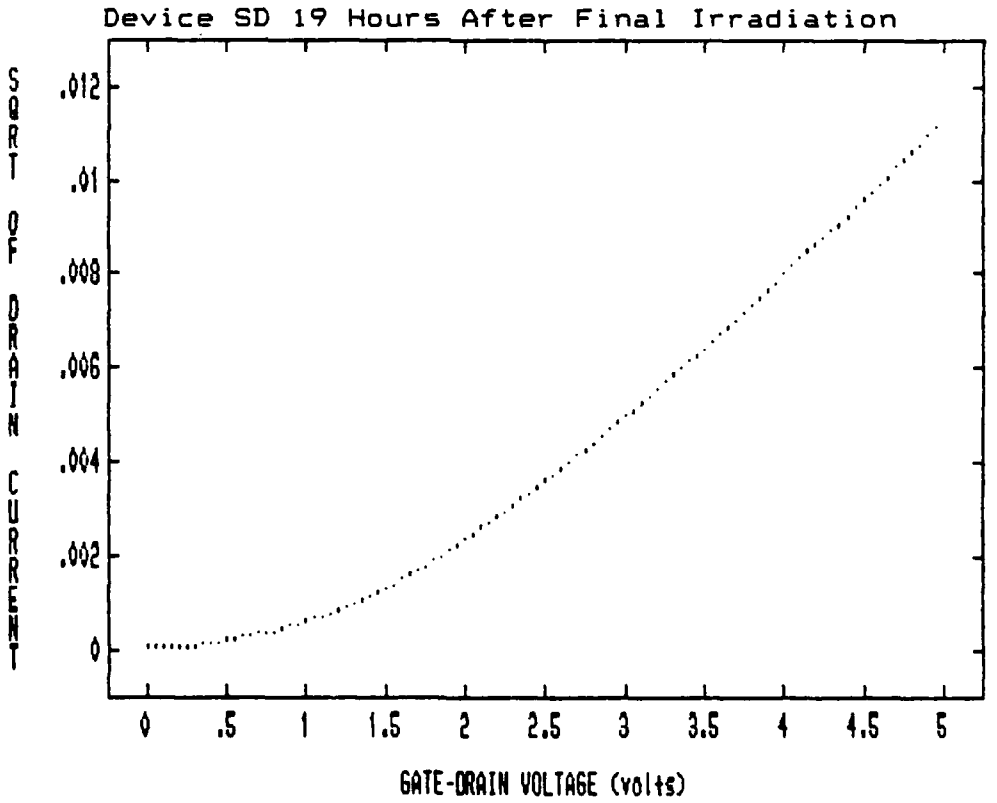


MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

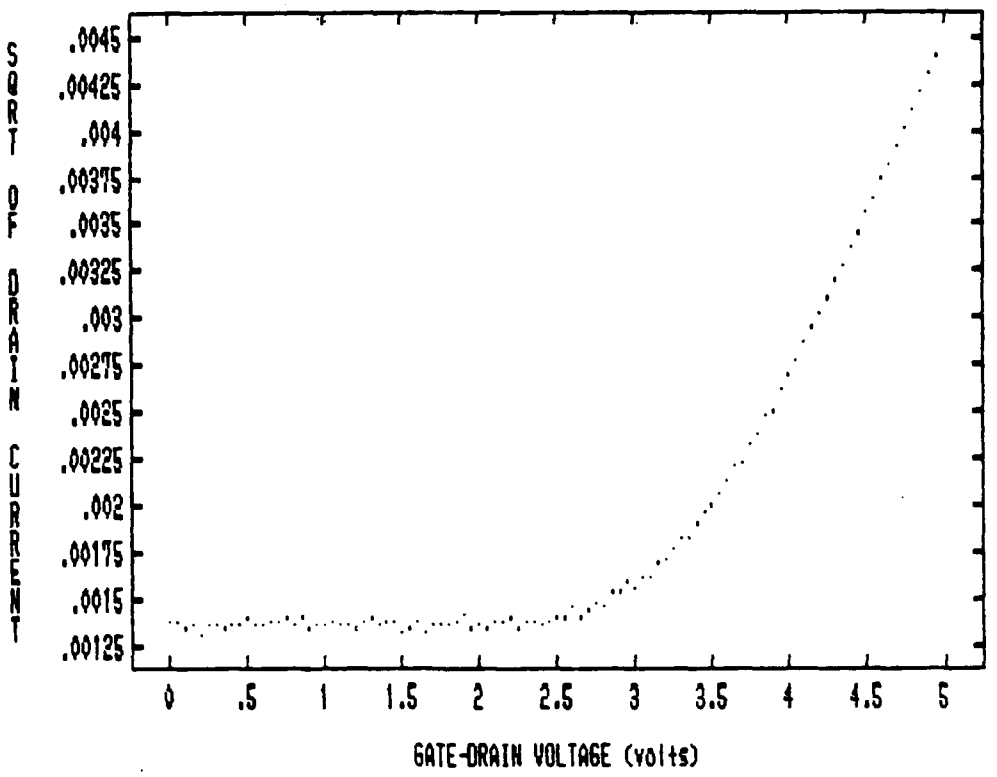




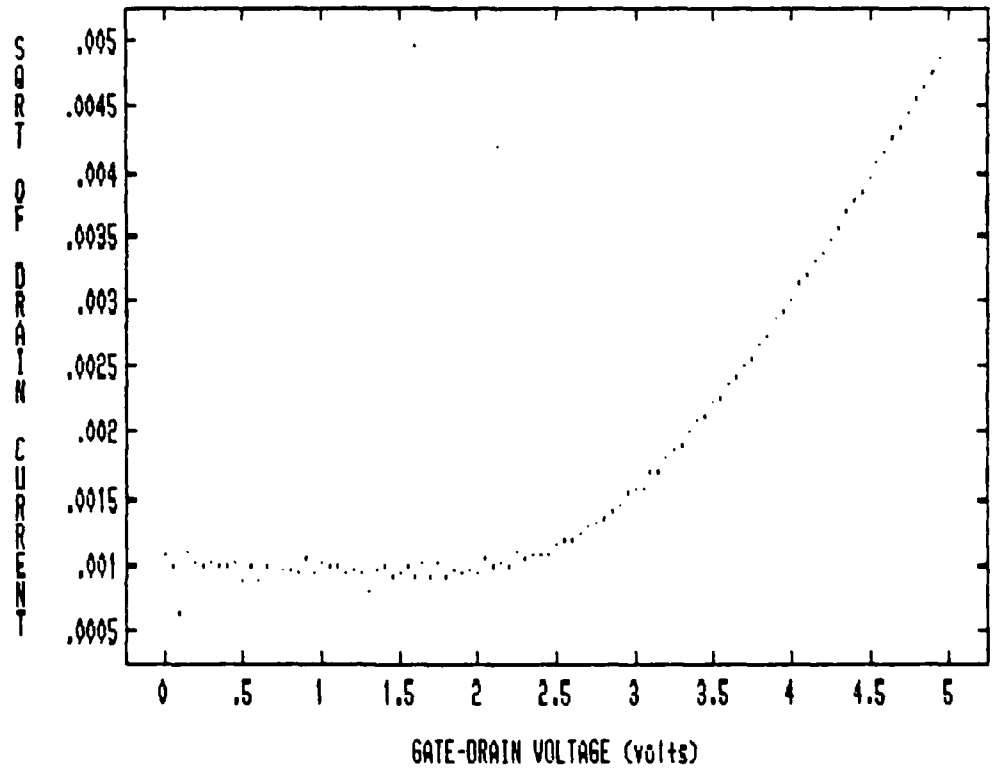


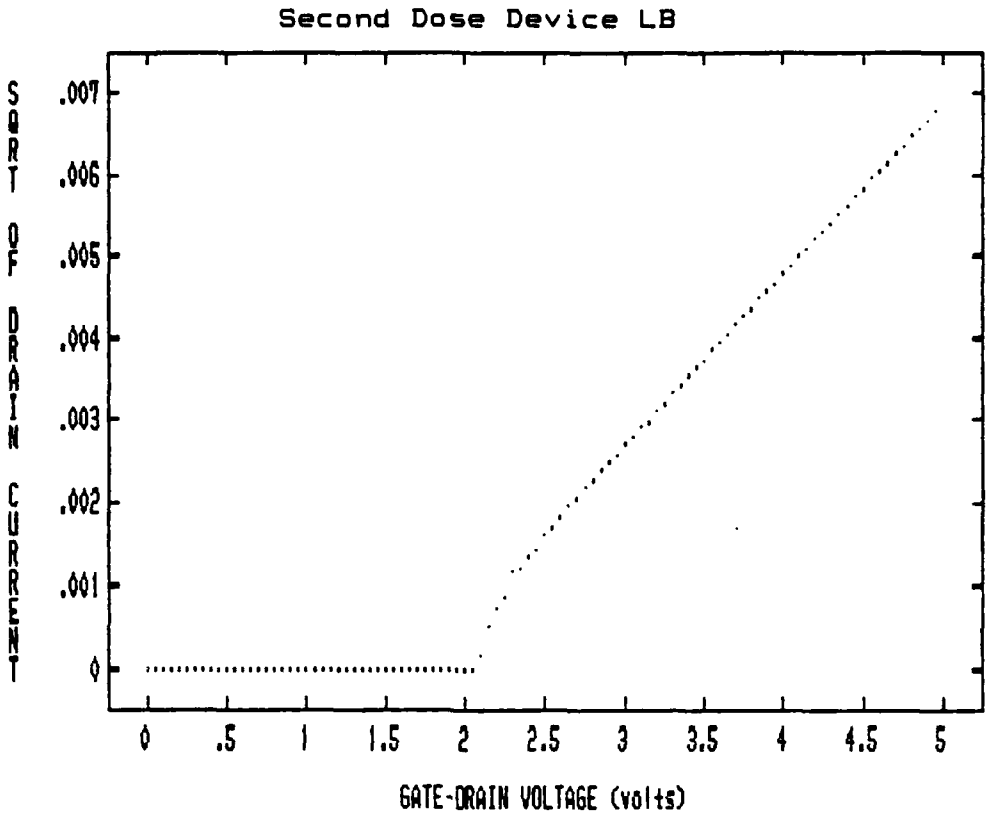


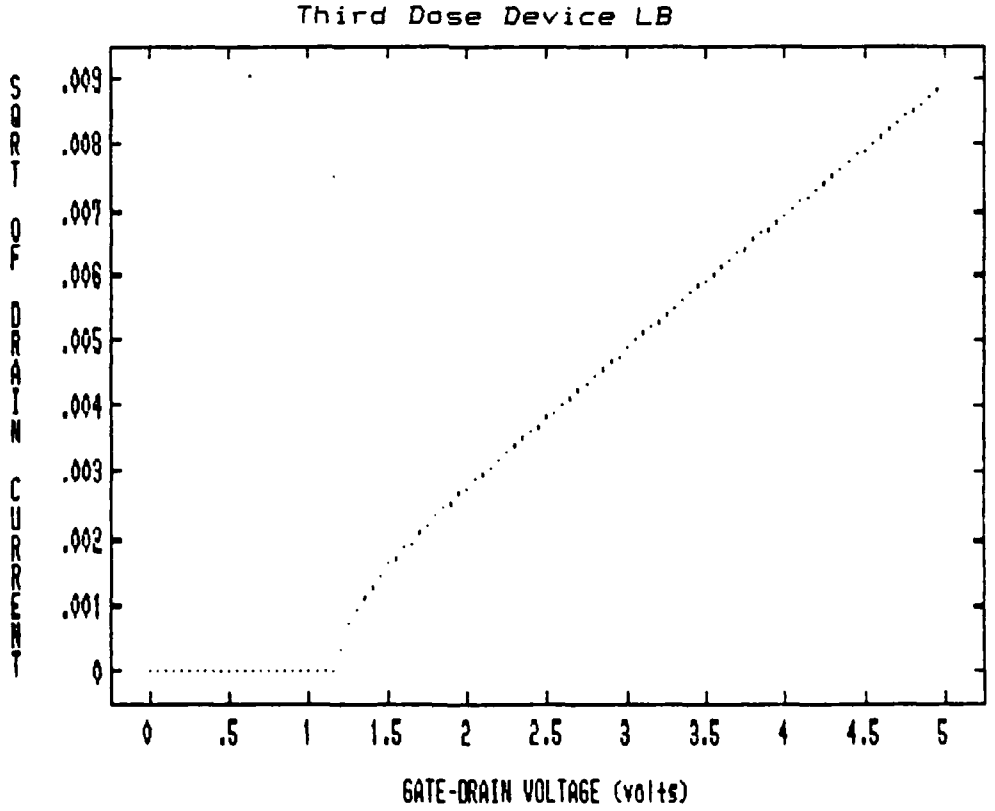
Pre-radiation Device LB



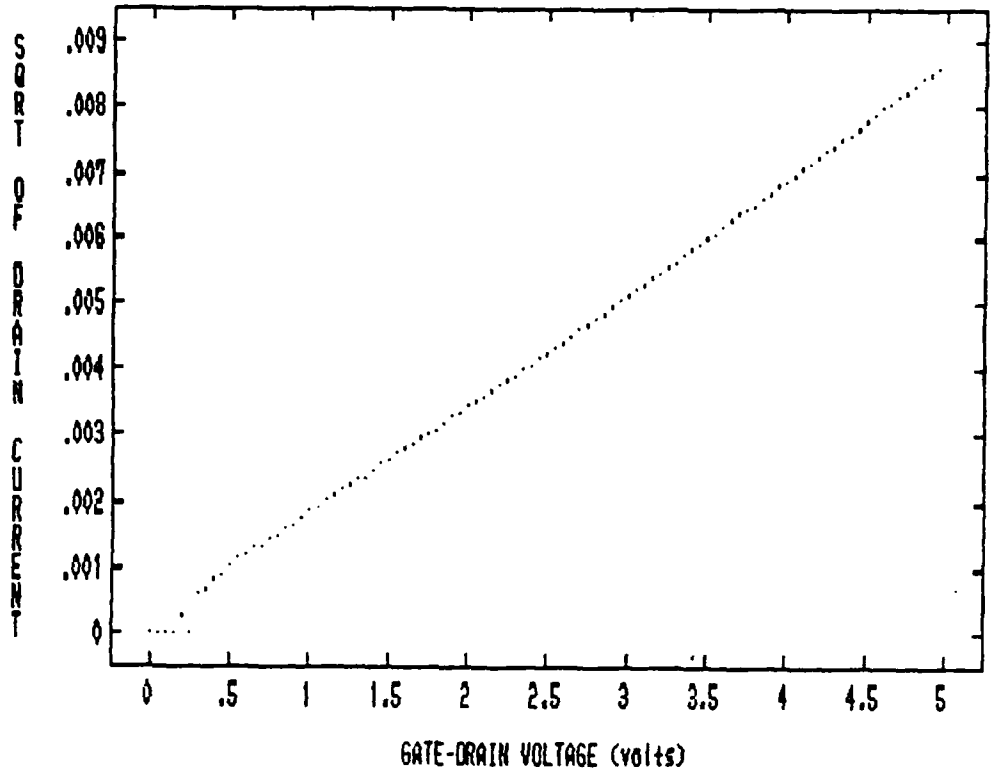
First Dose Device LB



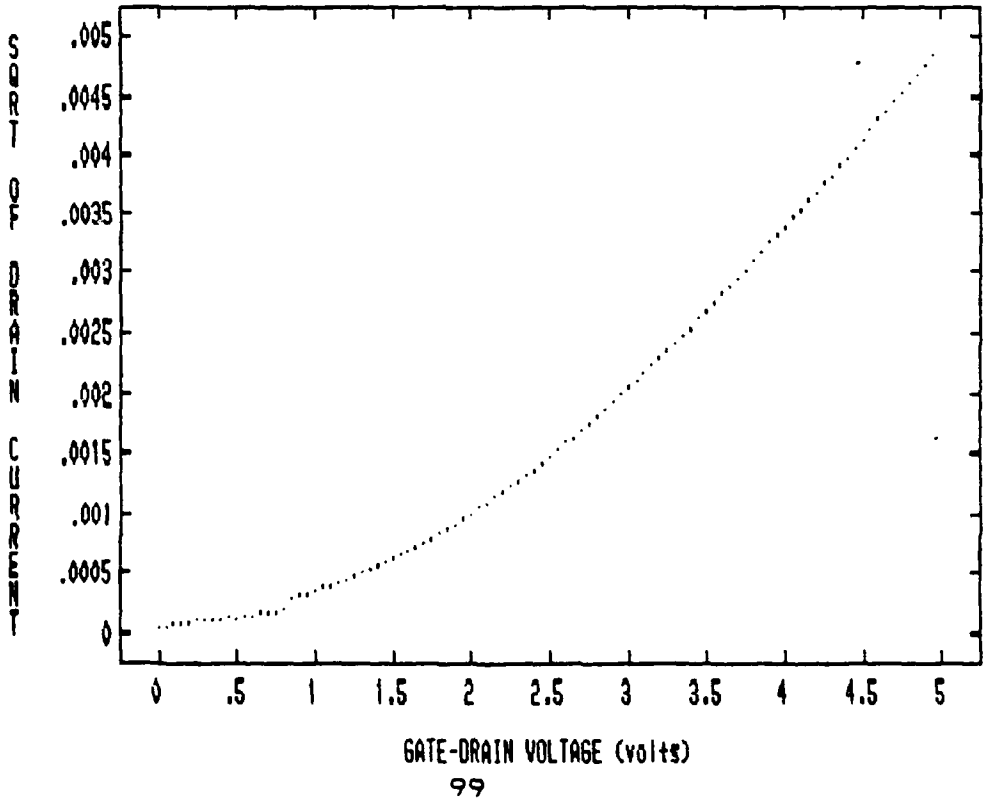




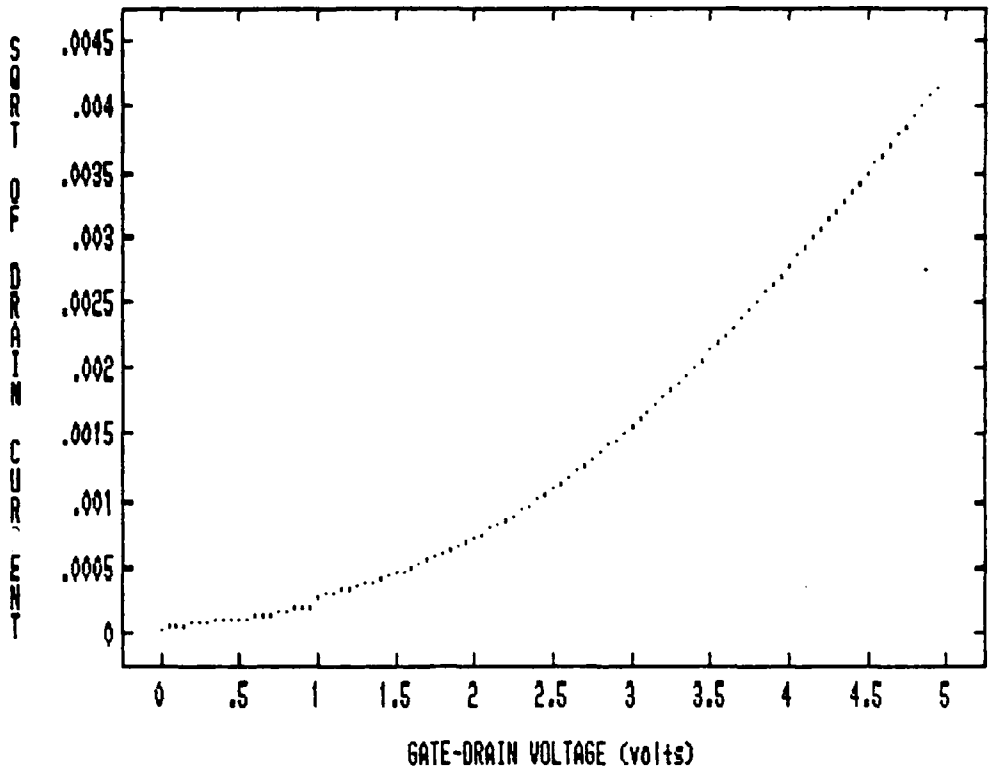
Fourth Dose Device LB



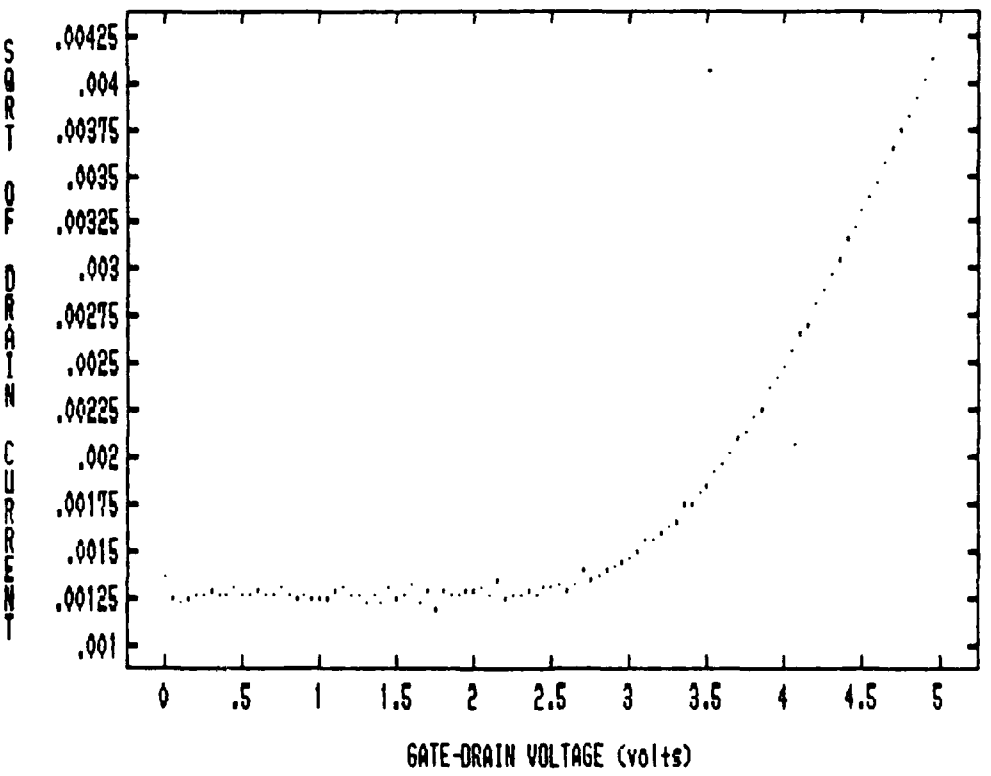
Device LB 27 Hours After Final Irradiation



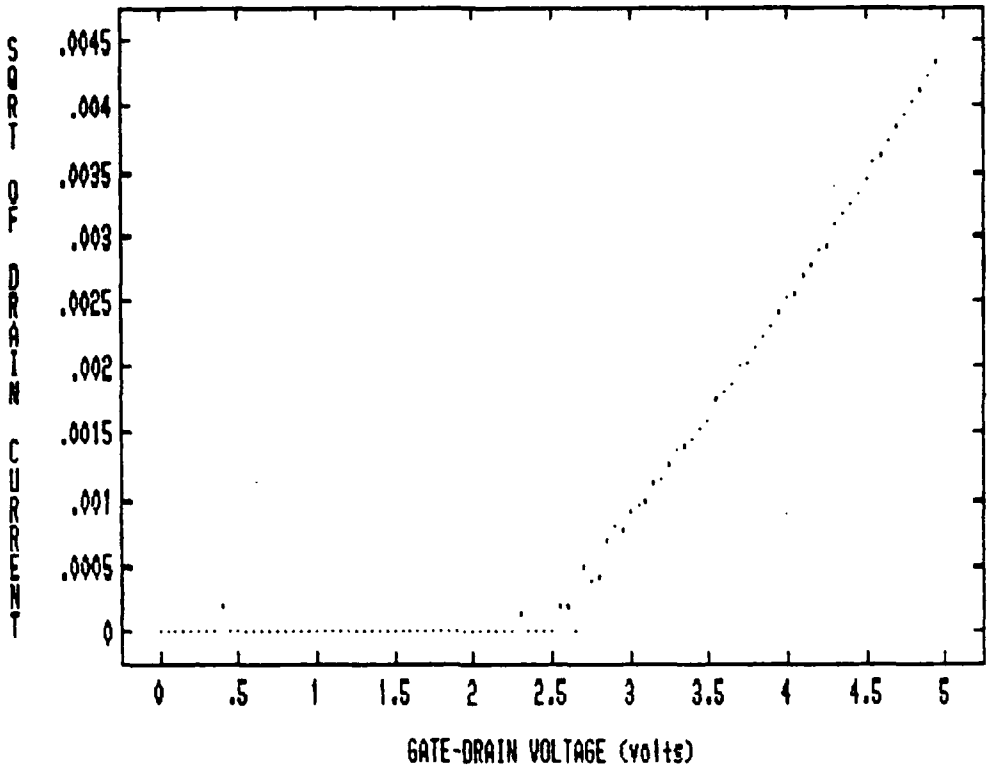
Device LB 59 Hours After Final Irradiation



Pre-radiation Device LC



First Dose Device LC



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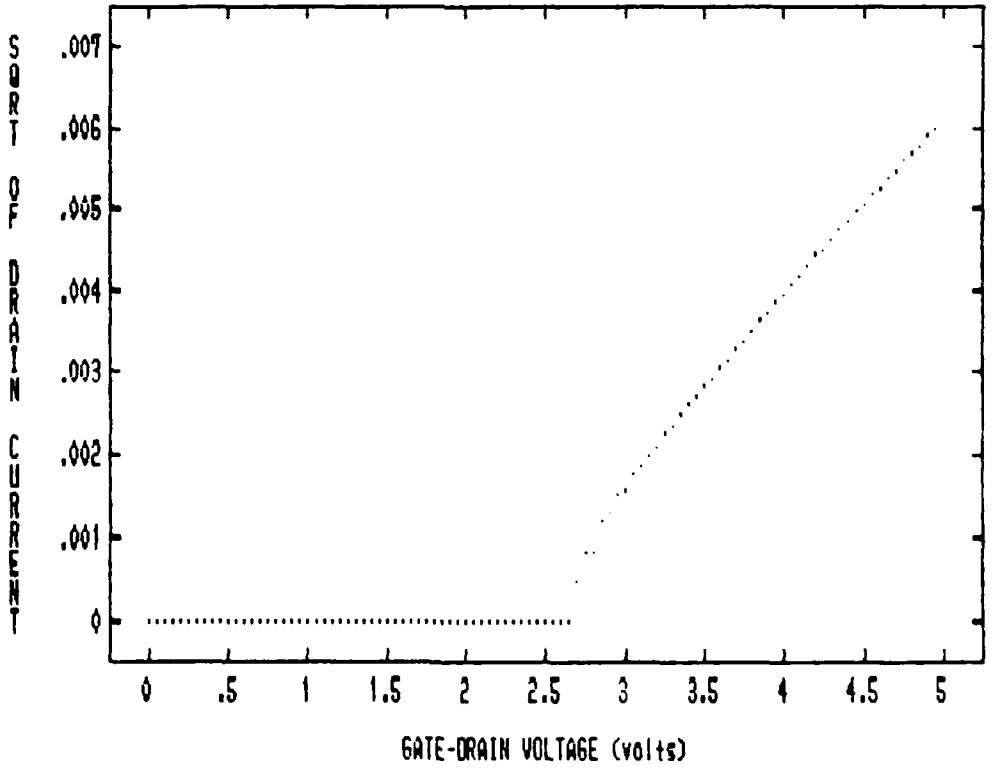
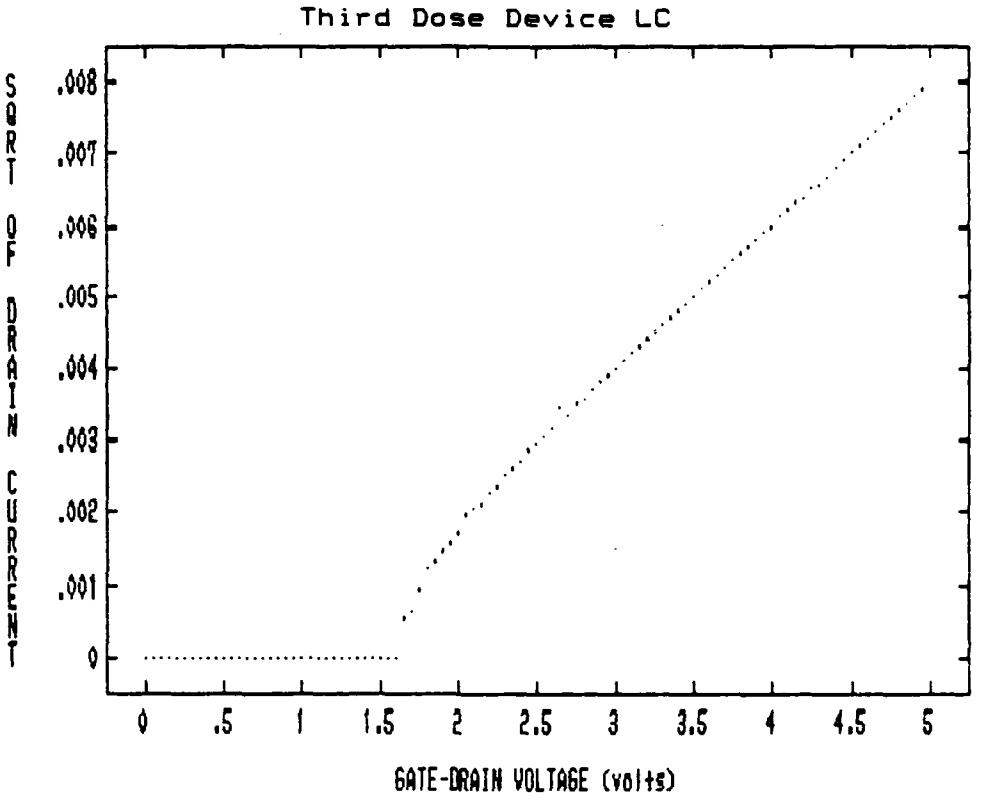
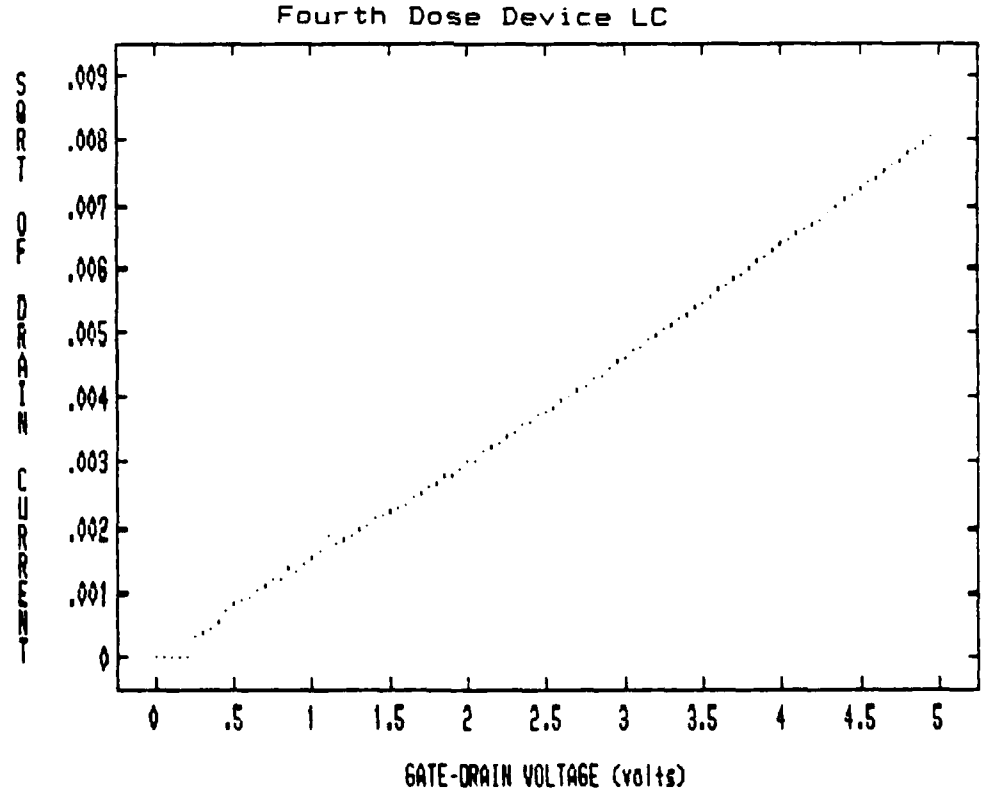
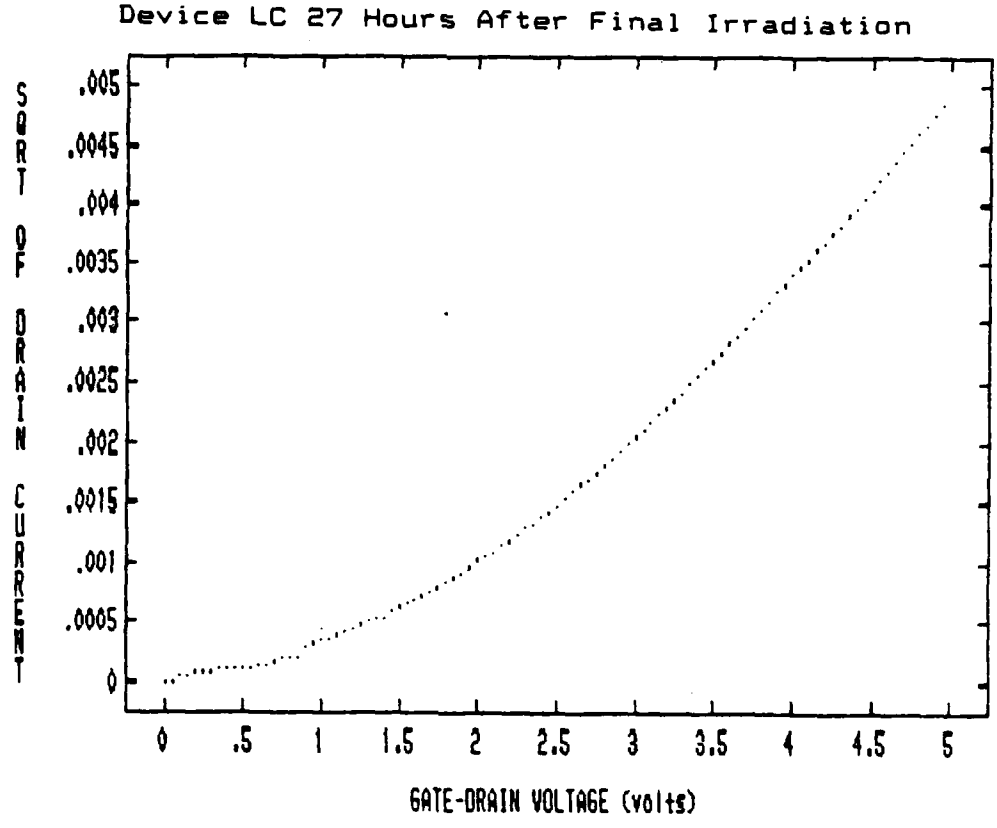
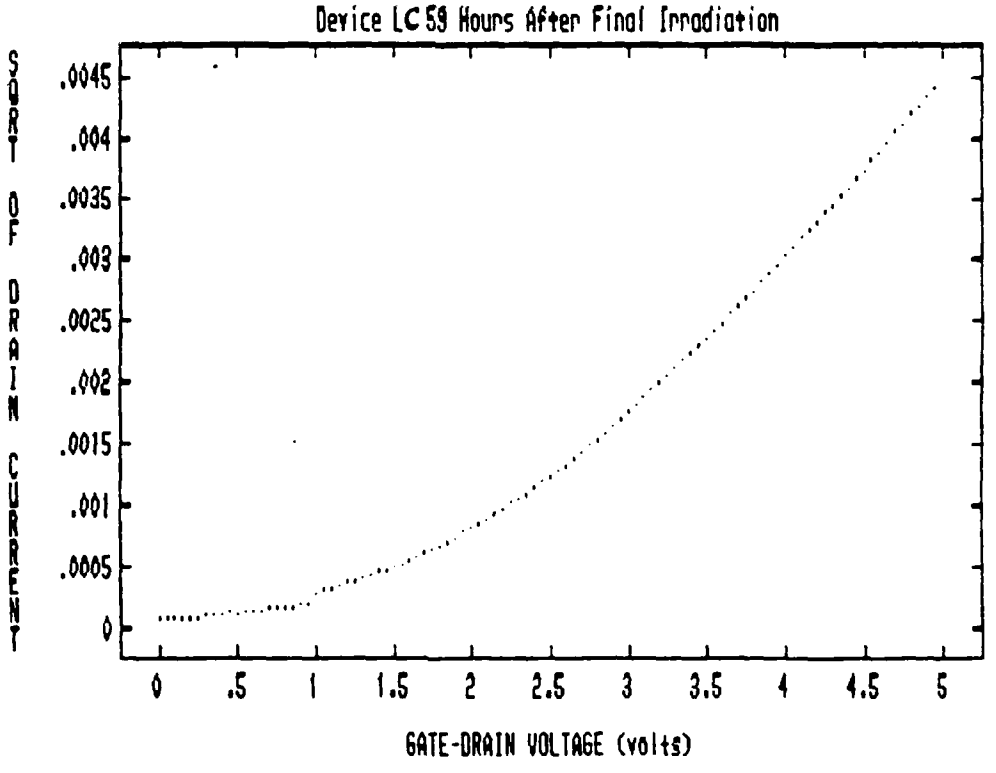
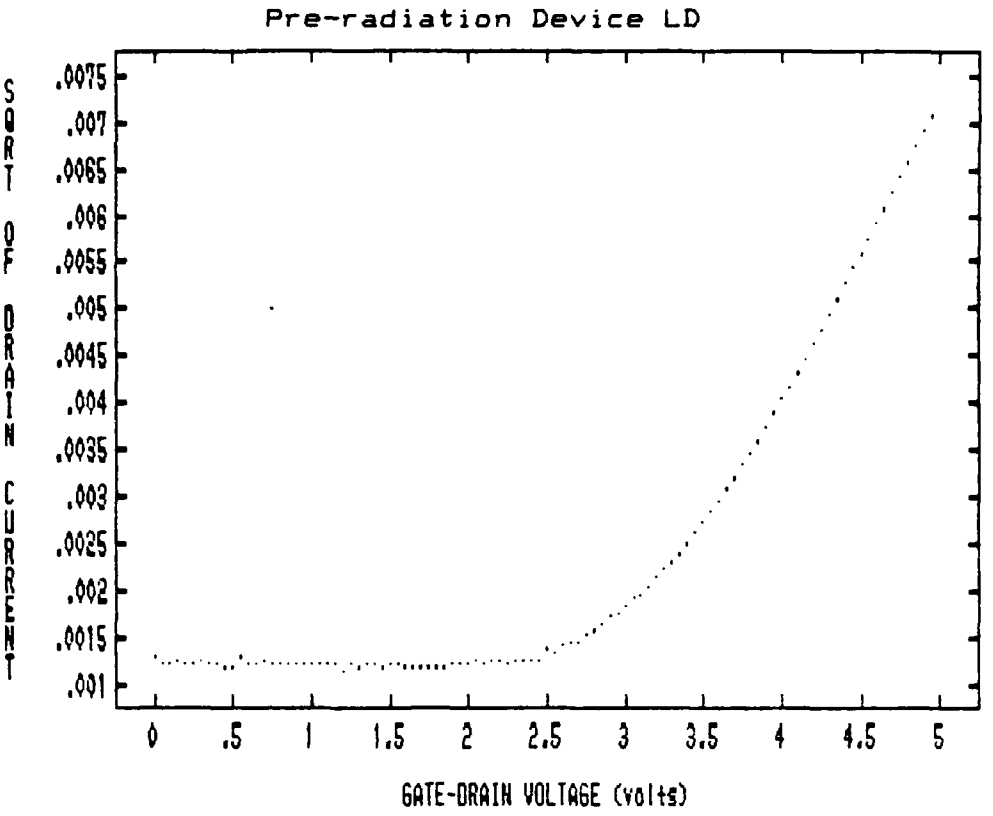


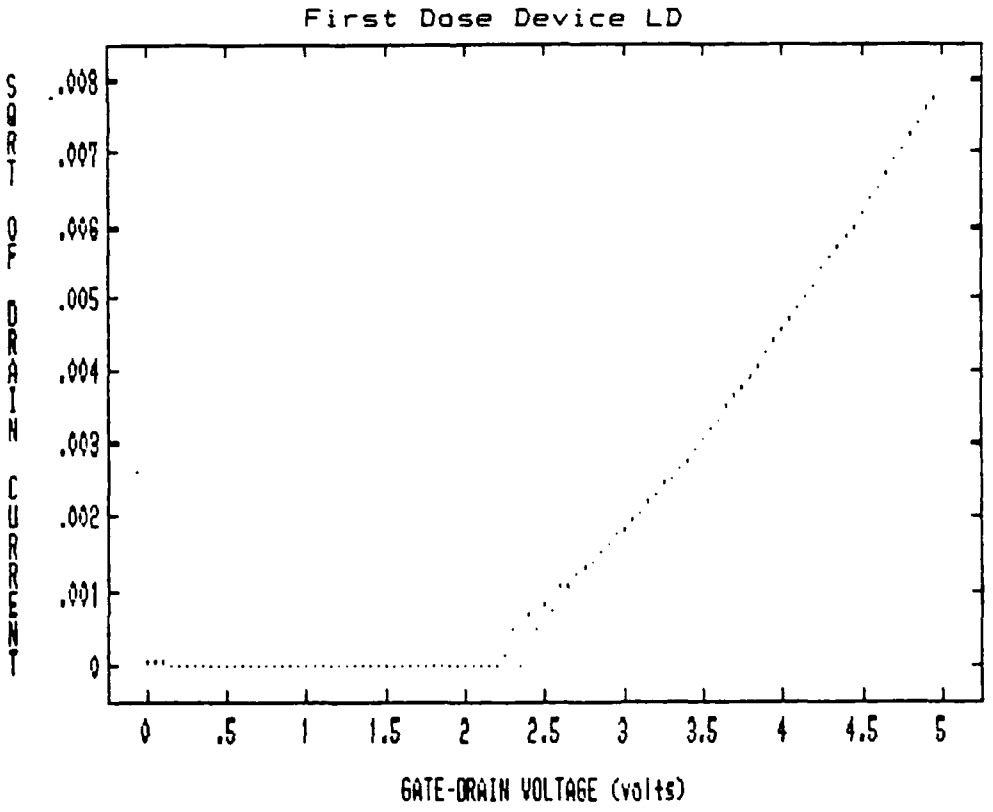


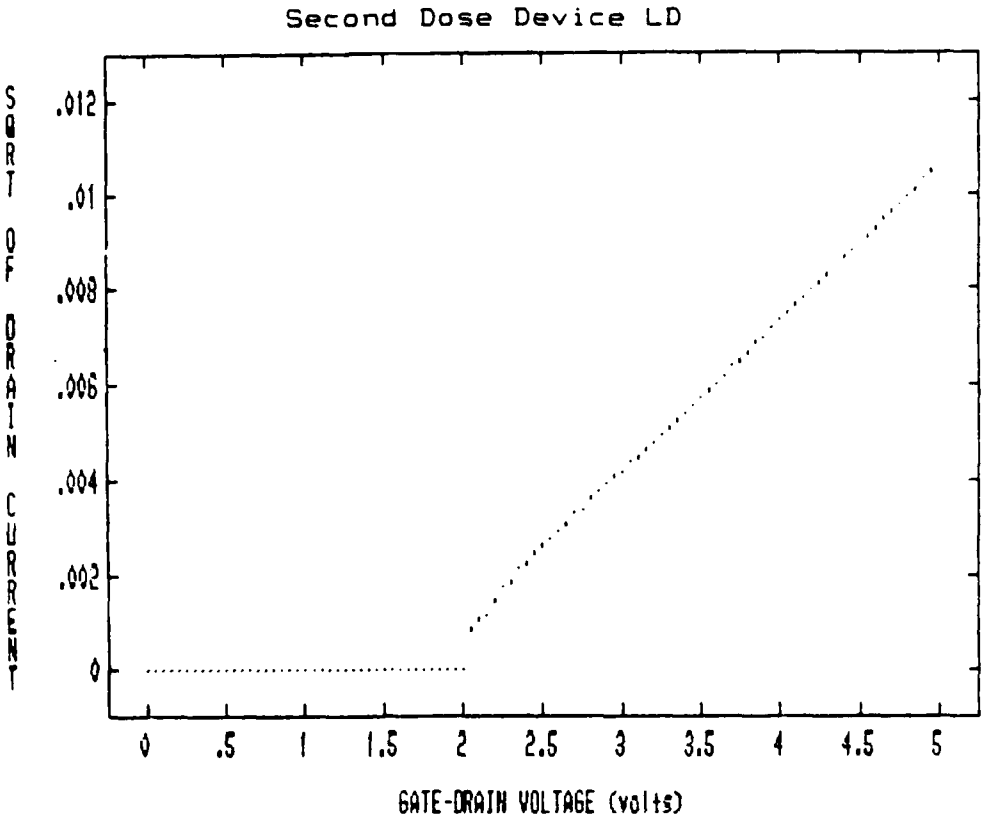


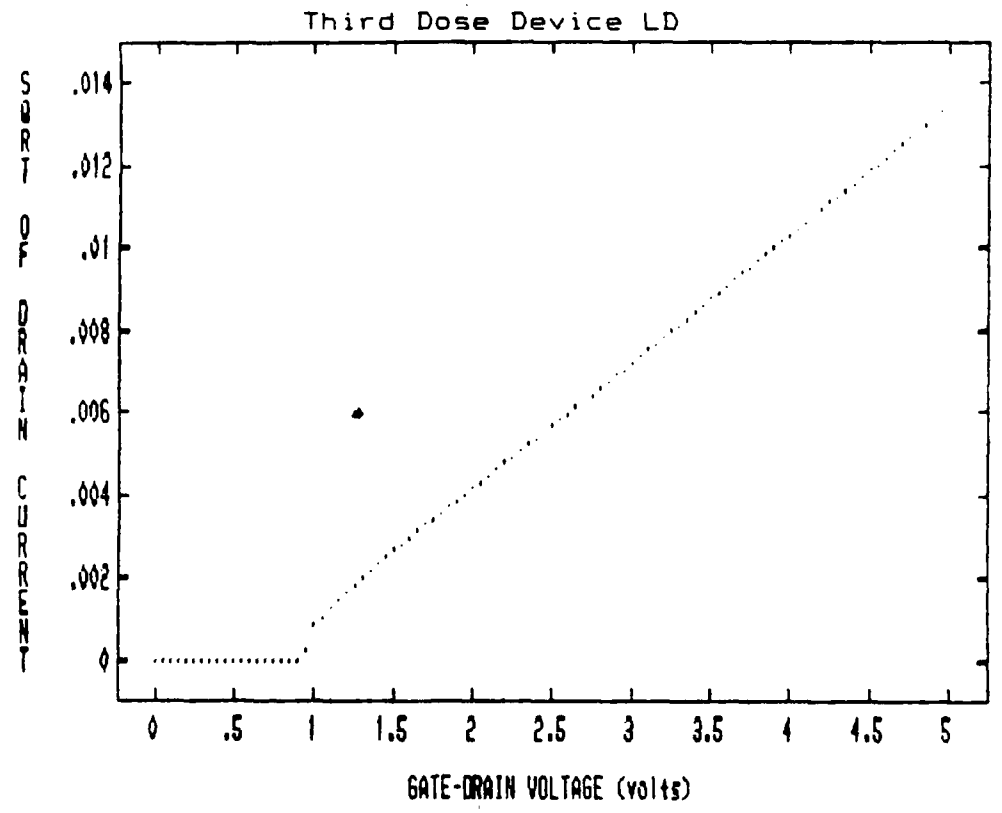


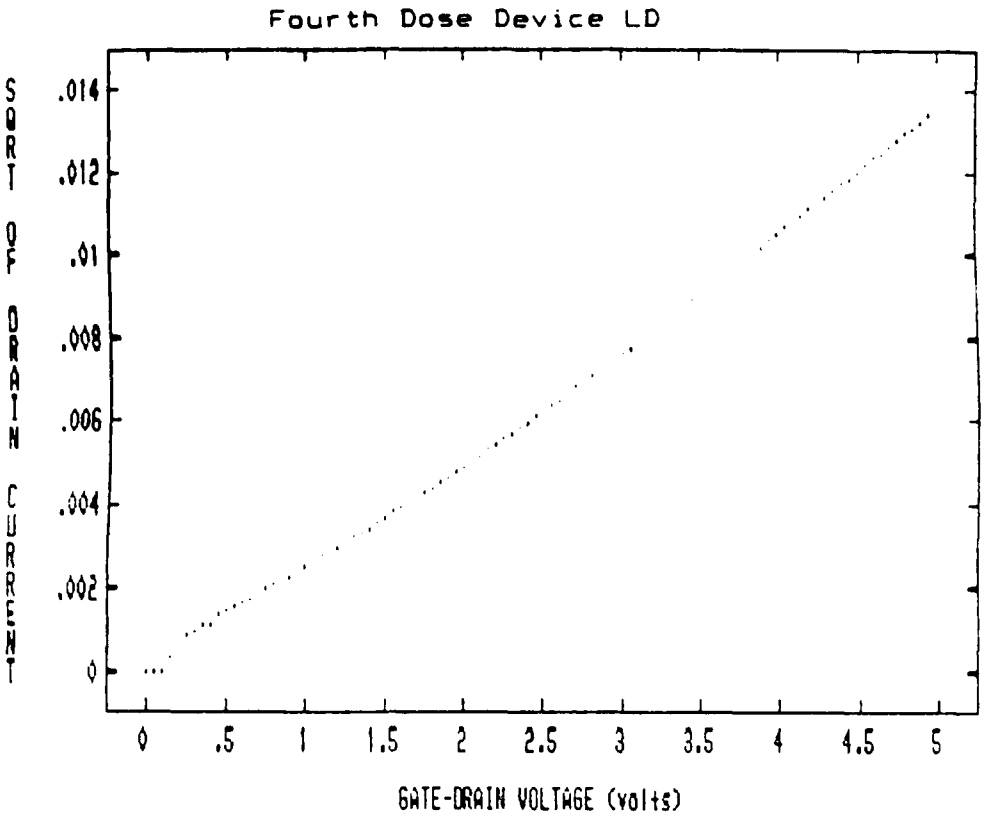


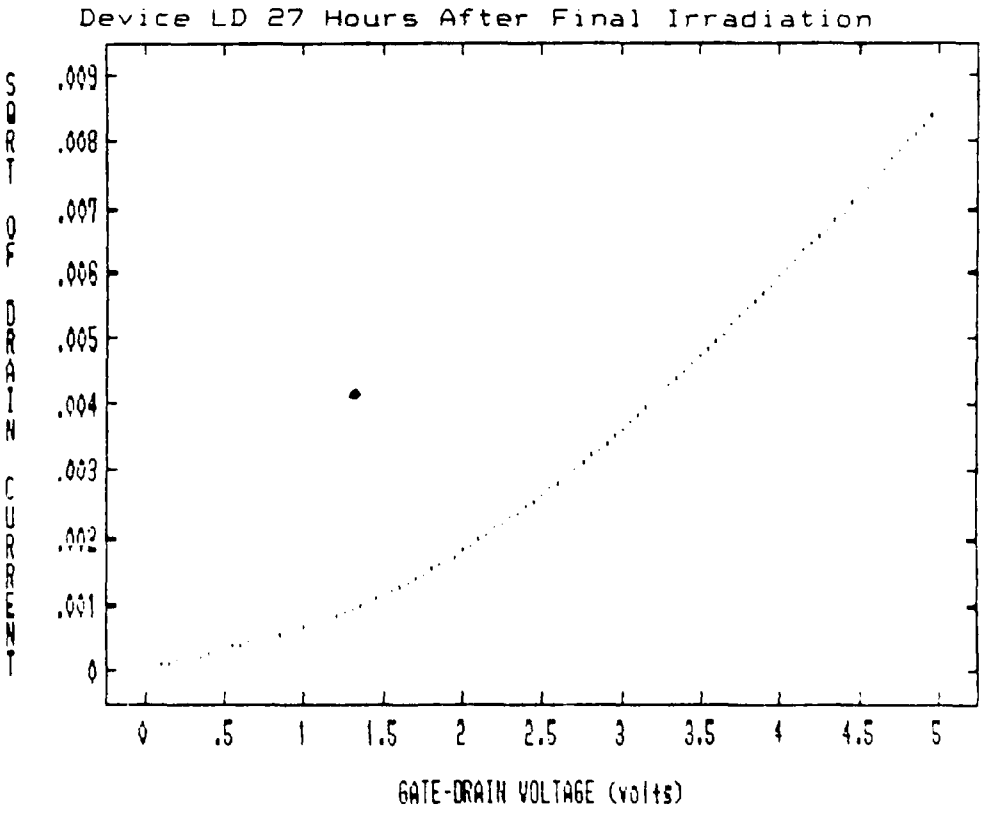


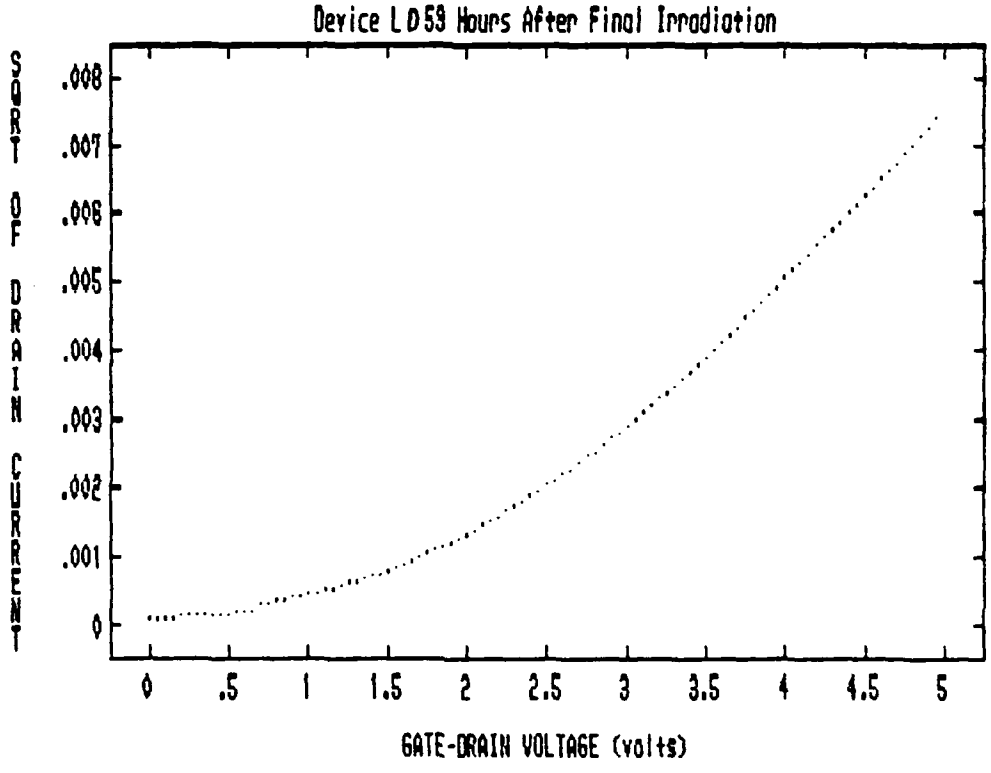







Fourth Dose Device LD
SQRT OF DRAIN CURRENT
.014
.012
.01
.008
.006
.004
.002
0
0
.5
1
1.5
2
2.5
3
3.5
4
4.5
5
GATE-DRAIN VOLTAGE (volts)


Device LD 27 Hours After Final Irradiation
SQRT OF DRAIN CURRENT
.009
.008
.007
.006
.005
.004
.003
.002
.001
0
0
.5
1
1.5
2
2.5
3
3.5
4
4.5
5
GATE-DRAIN VOLTAGE (volts)



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